

YouIP Portfolio 2021

A Leading Custom ASIC & IP Provider

Brite semiconductor

灿芯半导体（上海）股份有限公司

Brite Semiconductor (Shanghai) Co., Ltd.

Brite semiconductor

Brite's YouIP Portfolio

Advanced and Comprehensive
"YOU" IP Portfolio and Silicon Platform Solution



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BRITE'S YouIP PORTFOLIO

IP Name/Type	IP Code	Process	Description	Maturity
YouPHY-USB	B14SFP_USB20_PHY	14nm SF+	USB2.0 OTG PHY	Silicon Proven
	B28HKCP_USB20_PHY	28nm HKC+	USB2.0 OTG PHY	Silicon Proven
	B40NLL_USB20_PHY	40nm LL	USB2.0 OTG PHY	Silicon Proven
	B55NLL_USB20_PHY	55nm LL	USB2.0 OTG PHY	Silicon Proven
	B55NEF_USB20_PHY	55nm EF	USB2.0 OTGPHY	Silicon Proven
	B55PFULP_USB11	55nm ULP	USB1.1 PHY	Silicon Proven
	B011_USB20_PHY	0.11G	USB2.0 OTG PHY	Silicon Proven
	B013_ USB20_PHY	0.13G	USB2.0 OTG PHY	Silicon Proven
	B013EF_ USB20_PHY	0.13um embedded flash	USB2.0 OTG PHY	Silicon Proven
YouPHY-DDR	B14SFP_DDR45_PHY	14nm SF+	DDR4/DDR5 combo PHY up to 4800 Mbps	Paper
	B14SFP_DDR34LPDDR34	14nm SF+	DDR3, 4/LPDDR3,4 combo PHY up to 3200 Mbps	Silicon Proven
	B14SFP_DDR4LPDDR34	14nm SF+	DDR 4/LPDDR3,4 combo PHY up to 4266 Mbps	Silicon Proven
	B28HKCP_DDR34LPDDR34	28nm HKC+	DDR3, 4/LPDDR3,4 combo PHY up to 2667 Mbps	Silicon Proven
	B40NLL_DDR34LPDDR23	40nm LL	DDR3/DDR3U/DDR3L/DDR4/LPDDR2/LPDDR3 combo PHY	Silicon Proven
	B40NLL_DDR23LPDDR23	40nm LL	DDR2/DDR3/LPDDR2/LPDDR3 combo DDR PHY	Silicon Proven
	B55NLL_DDR4	55nm LL	DDR4 PHY	Silicon Proven
	B55NLL_DDR23LPDDR23	55nm LL	DDR2,3/LPDDR2,3 combo DDR PHY	Silicon Proven
YouPHY-SerDes	B14SFP_SERDES_32G	14nm SF+	1.25 Gb/s-32Gb/s multi-rate SerDes	Paper
	B28NHKP_SERDES	28nm HKC+	2.5 /5 /8 /16 Gb/s multi-rate SerDes	Silicon Proven
	B40NLL_SERDES	40nm LL	12.5 Gb/s multi-rate SerDes	Silicon Proven
	B40NLL_SERDES	40nm LL	1.25Gb/s-12.5Gb/s multi-rate SerDes	Silicon Proven
YouPHY-PCIe	B14SFP_PCIE5_PHY	14nm SF+	PCIE Gen5 PHY	Paper
YouSecure	Bsecure-PUF	NA	Physical Uncloneable Function	Silicon Proven
	Bsecure-AS	NA	Active Shield	Silicon Proven
	Bsecure-DS	NA	Digital Sensor	Silicon Proven
	Bsecure-TRNG	NA	All Digital True Random Number Generator	Silicon Proven
	Bsecure-DRBG	NA	Deterministic Random Bit Generator	Silicon Proven
YouCrypto	Bcrypto-AES	NA	Multi Mode AES Engine, ECB/CBC/CTR/OFB etc	Silicon Proven
	Bcrypto-DES	NA	DES/3DES Engine	Silicon Proven
	Bcrypto-HASH	NA	MD5,SHA1,SHA2 Engine	Silicon Proven
	Bcrypto-SHA3	NA	SHA3 Engine	Silicon Proven
	Bcrypto-PKE	NA	Public Key Engine,ECC,RSA,ECDH,ECDSA	Silicon Proven
	Bcrypto-Chacha	NA	Chacha20,Poly1305 Engine	Silicon Proven
	Bcrypto-Snow3G	NA	Snow3G Engine	Silicon Proven
	Bcrypto-KASUMI	NA	KASUMI Engine	Silicon Proven
	Bcrypto-SM2	NA	OSCCA, SM2 Engine	Silicon Proven
	Bcrypto-SM3	NA	OSCCA, SM3 Engine	Silicon Proven
	Bcrypto-SM4	NA	OSCCA, Multi Mode SM4 Engine, ECB/CBC/CTR/OFB etc	Silicon Proven
	Bcrypto-SM9	NA	OSCCA, SM9 Engine	Silicon Proven
	Bcrypto-ZUC	NA	OSCCA, ZUC Engine	Silicon Proven

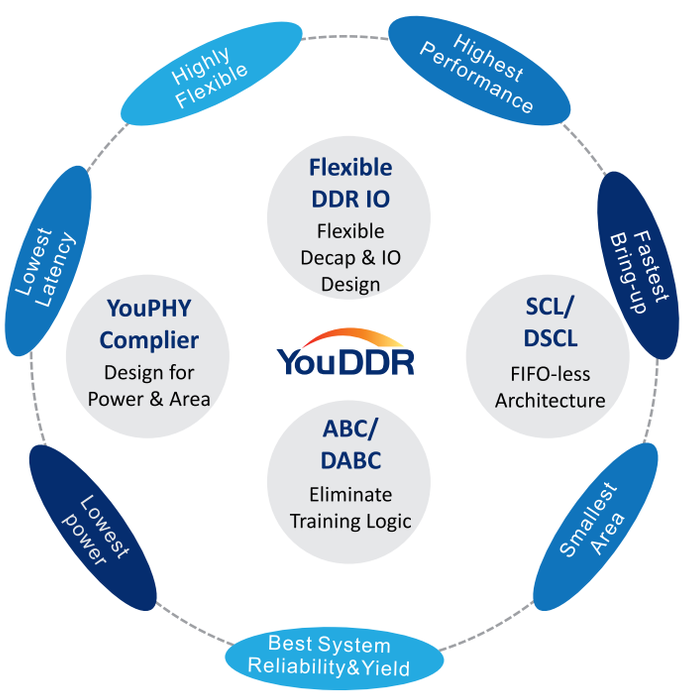
IP Name/Type		IP Code	Process	Description	Maturity
YouCrypto		Bcrypto-Coprocessor	NA	TRNG,DRBG and all the crypto engines, except for high throughput	Silicon Proven
		Bcrypto-AES-GCM/CTR	NA	Very High Throuput AES Engine, GCM/CTR Mode	Silicon Proven
		Bcrypto-AES-XTS	NA	Very High Throuput AES Engine, XTS Mode	Silicon Proven
		Bcrypto-SM4-GCM/CTR	NA	OSSCA, Very High Throuput SM4 Engine, GCM/CTR Mode	Silicon Proven
		Bcrypto-SM4-XTS	NA	OSSCA, Very High Throuput AES Engine, XTS Mode	Silicon Proven
		Bcrypto-ChaCha-HP	NA	Very High Throuput Chacha20-Poly1305 Engine	Silicon Proven
		Bcrypto-MultiPKE	NA	Multiple PKE Engines + Scheduler	Silicon Proven
		Bcrypto-MultiSM2	NA	OSCCA, Multiple SM2 Engines + Scheduler	Silicon Proven
YouRF-BLE		B55NLL_BLE	55nm LL	BLE_TRX plus LDO/DCDC PLUS IO	Paper
YouPHY-ONFI		B14SFP_ONFI5_PHY	14nm SF+	ONFI5.0 NAND Flash PHY	Paper
		B14SFP_ONFI4_PHY	14nm SF+	ONFI4.2 NAND Flash PHY	Paper
		B40NLL_ONFI4_PHY	40nm LL	ONFI4.0 NAND Flash PHY	Silicon Proven
YouPHY-MIPI		B14SFP_MIPI_DPHY	14nm SF+	2.5Gbps TX, RX MIPI 2.1 DPHY	Silicon Proven
		B40NLL_MIPI_DPHY	40nm LL	2.5Gbps TX , RX MIPI 2.1 DPHY	Silicon Proven
YouIO		B14SFP _DDRIO_DDR45	14nm SF+	DDR combo IO support DDR4/DDR5	Paper
		B14SFP_DDRIO_D4LP34	14nm SF+	DDR combo IO support DDR4/LPDDR3,4	Silicon Proven
		B14SFP_DDRIO_D34LP34	14nm SF+	DDR combo IO support DDR3,4/LPDDR3,4	Silicon Proven
		B28HKCP_DDRIO_D34LP34	28nm HKC+	DDR combo IO support DDR3,4/LPDDR3,4	Silicon Proven
		B40NLL_DDRIO_D34LP23	40nm LL	DDR combo IO support DDR3,3U,3L,4/LPDDR2,3	Silicon Proven
		B40NLL_DDRIO_COMBO	40nm LL	DDR combo IO support DDR2,3/LPDDR2,3	Silicon Proven
		B55NLL_DDRIO_D4	55nm LL	DDR IO support DDR4	Silicon Proven
		B55NLL_DDRIO_COMBO	55nm/65nm LL	DDR combo IO support DDR2/3/3L /LPDDR2/3	Silicon Proven
		B14SFP_ONFI5_IO	14nm SF+	ONFI5.0 NAND Flash IO	Paper
		B14SFP_ONFI4_IO	14nm SF+	ONFI4.2 NAND Flash IO	Silicon Proven
		B40NLL_ONFI4_IO	40nm LL	ONFI4.0 NAND Flash IO	Silicon Proven
		B14SFP_LVDS_IO	14nm SF+	LVDS IO	Paper
		B28NHKP_LVDS	28nm HKC+	LVDS IO	Silicon Proven
		B40NLL_LVDS	40nm LL	LVDS IO	Silicon Proven
YouAnalog	ADC	B14SFP_SARADC_12B100M	14nm SFP+	12bit 100MSPS 0.9V SAR ADC	Silicon Proven
		B28HKCP_SARADC_12B100M	28nm HKCP	12bit 100MSPS 0.9V SAR ADC	Silicon Proven
		B40NLL_ADC_V2512B5M	40nm LL	2.5/1.1V 12bit 5MSPS SAR ADC	Silicon Proven
		B40NLL_ADC_V2512B12M	40nm LL	2.5/1.1V 12bit 12MSPS SAR ADC	Silicon Proven
		B40NLL_ADC_V2512B2P5M	40nm LL	2.5/1.1V 12bit 2.5MSPS SAR ADC	Silicon Proven
		B40NLL_PIPADC_V1212B170M	40nm LL	12bit 170Msps pipeline ADC	Silicon Proven
		B40NLL_ADC_V3312B500K16CH	40nm LL	3.3V/1.2V 12bit 16channel 500KSPS SAR ADC	Silicon Proven
		B55NLL_PIPADC_V1212B100M	55nm LL	12bit 100Msps pipeline ADC	Silicon Proven
		B55NLL_ADC_V3310B100K	55nm LL	3.3/1.2V 10bit 100KSPS SAR ADC	Silicon Proven
		B55NLL_ADC_V1212B5M	55nm LL	3.3V/1.2V 12bit 5MSPS SAR ADC	Silicon Proven
		B55NLL_ADC_V1212B25M	55nm LL	3.3V/1.2V 12bit 25MSPS SAR ADC	Silicon Proven
		B55PFULP_ADC_V1210B16M	55nm ULP	1.2V 10bit 16MSPS SAR ADC	Silicon Proven

IP Name/Type		IP Code	Process	Description	Maturity
YouAnalog	ADC	B55NEF_ADC_V3312B2P5M	55nm EF	1.2V/3.3V 12bit 2.5MSPS SAR ADC	Silicon Proven
		B55NEF_ADC_V3316B1M	55nm EF	16bit 1MSPS SAR ADC	Silicon Proven
	DAC	B40NLL_DAC_V2512B12M	40nm LL	1.1V/2.5V 12bit 12MHz current steering DAC	Silicon Proven
		B40NLL_DAC_V3310B300M4CH	40nm LL	10bit 300MHz 4channel DAC	Paper
		B40NLL_IQDAC_V3312B170M	40nm LL	12bit 170MHz IQDAC	Silicon Proven
		B55NLL_DAC_V3312B100M	55nm LL	12bit 100MHz DAC	Silicon Proven
		B55NEF_DAC_V3312B100M	55nm EF	12bit 100MHz DAC	Silicon Proven
		B55PFULP_DAC_V128B16M	55nm ULP	8bit 16MHz DAC	Silicon Proven
	AUDIO_CODEC	B55NLL_AUDIO_CODEC	55nm LL	AUDIO CODEC	Silicon Proven
	BG	B40NLL_VBG_VR3311	40nm LL	1.1V voltage output	Silicon Proven
		B40NLL_BGP	40nm LL	1.1V/2.5V 1.25V voltage output and 10uA/5uA current output	Silicon Proven
		B55NEFV1836VBG2	55nm EF	1.2V/3.3V 1.23V voltage output and 20uA current output Bandgap	Silicon Proven
	Buck	B55PFULP_DCDC_V1836C10	55nm ULP	DCDC voltage converter	Silicon Proven
		B55PFULP_DCDC_V1836C15	55nm ULP	DCDC voltage converter	Silicon Proven
	LDO	S40NLLVR3311C240	40nm LL	Input 3.3V, output 1.1V, supply 240mA loading current(max), load 2.2uF cap (Typ)	Silicon Proven
		S40NLLVR3311C5	40nm LL	Input 3.3V, output 1.1V, supply 5mA loading current(max), load 40pF cap (Typ)	Silicon Proven
		B40NLL_VR_V3311C50	40nm LL	Input 1.62-3.63V, output 1.1V, supply 50mA loading current(max), load 4.7uF cap (Typ)	Silicon Proven
		B55NLL_VR1U_V3312C100U	55nm LL	Input 1.9-3.6V, output 1.2V, supply 100uA loading current(max)	Silicon Proven
		B55NEF_VR_V3318C30B	55nm EF	Input 3.3V, output 1.8V, supply 30mA loading current(max), load 100pF cap (Typ)	Silicon Proven
		B55PFULP_VR_V3318C30	55nm ULP	Input 2.3-3.63V, output 1.8V/1.2V, supply 10mA/20mA loading current(max), load 100pF cap (Typ)	Silicon Proven
		B55PFULP_CPLDO_2X	55nm ULP	Input 1.4V, output 2.4V, supply 2.5mA loading current(max), load 500pF cap (max)	Silicon Proven
	POR	B55NLL_POR_V12	55nm LL	Supply voltage : Vsup =1.2V~1.32V ; operation current: <0.1uA℃ operating junction temperature :-40℃ ~+25℃ ~+125℃	Silicon Proven
		B55NEF_POR_V33	55nm EF	Supply voltage : Vsup =1.7V~3.63V ; operation current: 57uA℃ operating junction temperature :-40℃ ~+25℃ ~+125℃	Silicon Proven
	OSC	B40NLLROSC_100M	40nm LL	100MHz ROSC	Silicon Proven
		B40NLL_XOSC_32K	40nm LL	Output frequency 32.768KHz:supply voltage:1.62V~3.6V:current consumption :507nA	Silicon Proven
	EEPROM	B130EE_EEPROM_2KB	130nm EE	2KByte EEPROM	Silicon Proven
	AFE	B55PFULP_AFE_QT	55nm ULP	Analog front end	Silicon Proven
YouSiP-IoT	Processor platform	B55NEFIoT	55nm EF	ARM Cortex M processor + EF + embedded PMU + Sensor interfaces + BLE connectivity	Silicon Proven
		B55NEFIoT_ARC	55nm EF/ULP	ARC+ EF+ BLE+ USB2.0+ ADC	Silicon Proven
		B95NULPIoT	95ULP	ARM Cortex M processor + MTP + embedded PMU + Sensor interfaces + BLE connectivity	Silicon Proven
YouSiP-Audio	DSP platform	B55NLLAudioDSP_CEVATL4	55nm LL	TL410 and peripherals for audio and sensor data processing	Silicon Proven
YouSiP-Vision	DSP platform	B28NHKVisionDSP_CEVAXM4	28nm HKMG		Silicon Proven
		B40NLLVisionDSP_CEVAXM4	40nm LL	Vision platform which consists of multiple instances of CEVA XM4 DSP processors, MIPI, PCIe and DDR interfaces. The platform enables three key elements of intelligent vision processing: 3D vision, computational photography, visual perception and analytics.	Silicon Proven
YouSiP-AP	Processor Platform	B28NHKCPU	28nm HKMG	Storage platform with DDR interface. Harden ARM Cortex A9 dual-core 32K/32K I/D Cache + Neon/FPU + CoreSight + Snoop Hard Core	Silicon Proven
		BCPU_ARMCA9_DC_40LL_V1	40nm LL	Harden ARM Cortex A9 dual-core 32K/32K I/D Cache + Neon/FPU + CoreSight + Snoop Hard Core	Silicon Proven

YouDDR

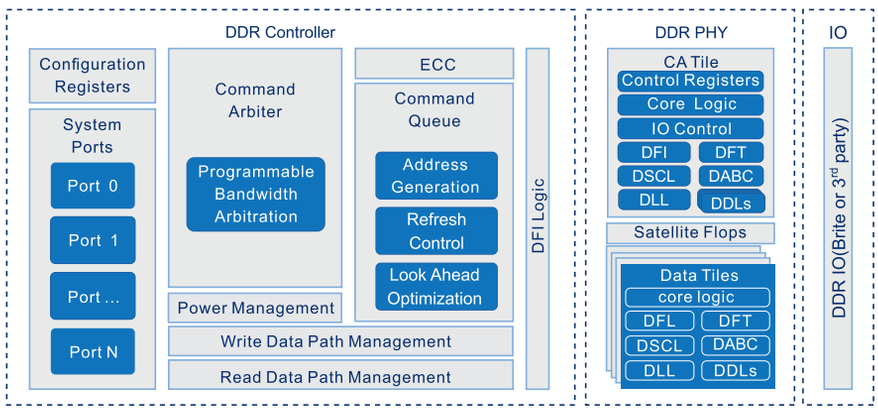
HIGH SPEED DDR INTERFACE SOLUTION

DDR Code	Process	DDR2 (Mbps)	DDR3 (Mbps)	DDR4 (Mbps)	DDR5 (Mbps)	LPDDR2 (Mbps)	LPDDR3 (Mbps)	LPDDR4 (Mbps)	Maturity
B14SFP_DDR45	14nm SF+	--	--	3200	4800	--	--	--	Paper
B14SFP_DDR4LPDDR34	14nm SF+	--	--	3200	--	--	2133	4266	Silicon Proven
B14SFP_DDR34LPDDR34	14nm SF+	--	2133	3200	--	--	2133	3200	Silicon Proven
B28HKCP_DDR34LPDDR34	28nm HKC+	--	2133	2666	--	--	2133	2666	Silicon Proven
B40NLL_DDR34LPDDR23	40nm LL	--	1866	1866	--	1066	1866	--	Silicon Proven
B40NLL_DDR23LPDDR23	40nm LL	1066	1333	--	--	1066	1066	--	Silicon Proven
B55NLL_DDR4	55nm LL	--	--	1866	--	--	--	--	Silicon Proven
B55NLL_DDR23LPDDR23	55nm LL	1066	1066	--	--	1066	1066	--	Silicon Proven



YouPHY-DDR Advanced Patented Technology

Brite provides a complete DDR subsystem including not only controller, PHY and IO, but also corresponding tuning and configuration software. And this solution can support LPDDR2, DDR3, LPDDR3, DDR4, LPDDR4 and DDR5 combo PHY with the data rate from 667Mbps to 4800Mbps. YouPHY-DDR is developed on 130um to 14nm process respectively and delivers an unbeatable combination of DDR high speed and low power performance. With patented dynamic self-calibrating logic (DSCL) and dynamic adaptive bit calibration (DABC) technology, YouPHY-DDR can automatically compensate chip/package/board/memory PVT variation and bit-bit skew. YouPHY-DDR delivers the highest DDR performance, the smallest area and the shortest time-to-market.



YouPHY-DDR Subsystem

KEY DDR SUBSYSTEM FEATURES

DDR Controller

- Highly flexible and customizable DFI 4.0 compliant DDR controller architecture
- Supports up to 32 target interfaces including AXI, AHB and FIFO-based interfaces
- User-customizable arbiter (scheduler)

DDR PHY

- Comprehensive DDR protocol training
  - CA training
  - DQ read training
  - DQ write training
  - Write leveling
  - Vref training
- PHY is DFI 4.0 compatible and backwards-compatible to earlier DFI standards for simplified integration with existing
  - DFI-compliant Controllers
- PHY includes DSCL technology
  - Automatically compensates for DDR interface timing due to static (process-related) variations and dynamic variations due to operating temperature, voltage, and data patterns
- PHY includes DABC technology
  - Automatically compensates for bit-bit skew within each byte lane
- DSCL delivers lowest PHY latency of 0.5 – 1 clock cycles
- Fast and simple system bring-up via DSCL hardware routine
- Improved long term system reliability
- Flexible, rectilinear PHY layout offers industry's smallest PHY area and is hardened to match IO pad frame
- PHY (and optionally IO) configured as drop-in hard macro for easy implementation

- Combo PHY options include:
  - DDR2/DDR3 PHY Combo
  - LPDDR2/DDR3 PHY Combo
  - LPDDR2/LPDDR3/DDR3 PHY Combo
  - DDR3/DDR4 PHY Combo
  - LPDDR3/4 + DDR4 PHY Combo
  - DDR4/DDR5 PHY Combo

DDR I/O

- High performance, low jitter DDR IO
- Low power / small footprint
- Silicon proven

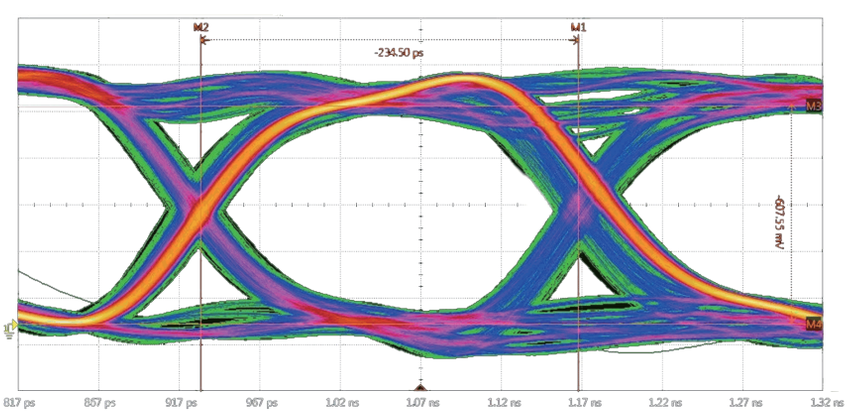
IP DELIVERABLES AND DESIGN SUPPORT

The DDR controller is delivered as RTL while the PHY and IO are delivered as hardened macros to fit the target chip floorplan and padframe. Brite can deliver a fully hardened DDR subsystem (controller, PHY and IO) if requested.

PHY Deliverables
Netlist, SDF, LEF, LIB, Verilog, timing reports, technical documentation.

IO Deliverables
All PHY deliverables padframe guidance and review.

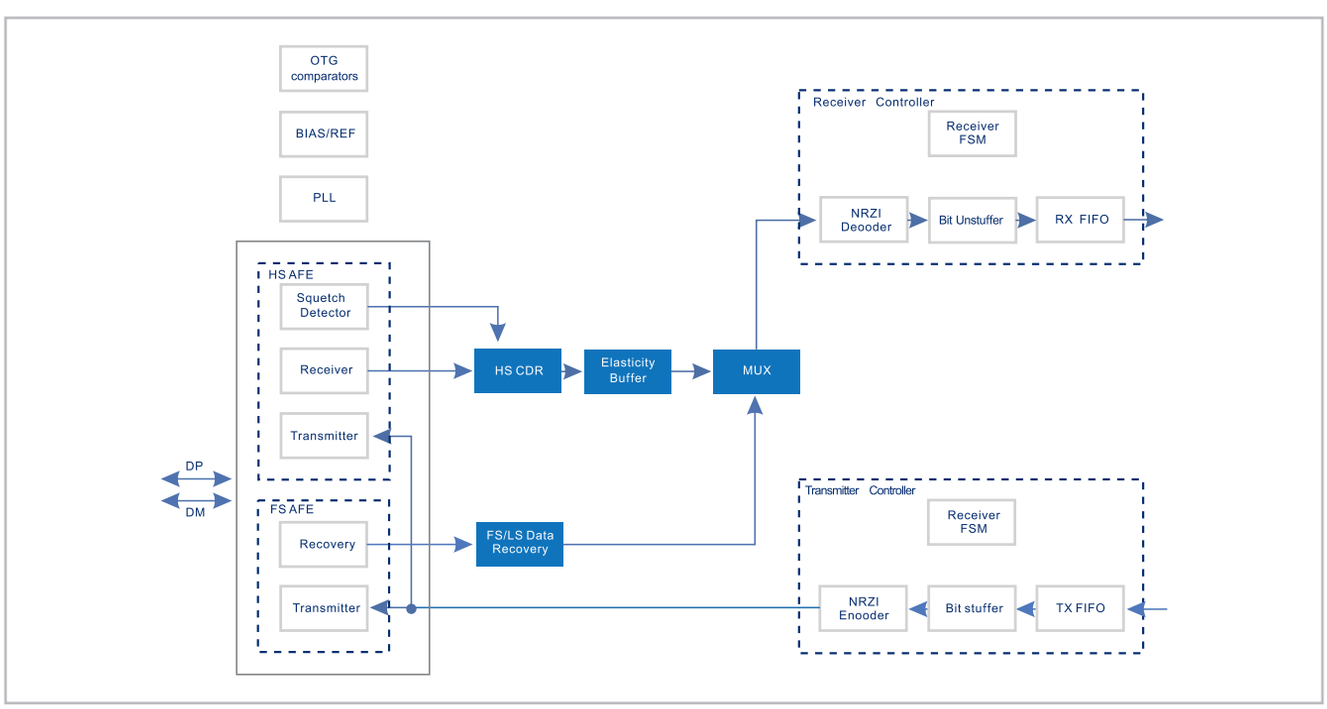
Technical Guidance
Brite provides complete layout and integration guidelines for the DDR IP and a technical review of the DDR subsystem implementation prior to tapeout. Support is also available for silicon bring up.



LPDDR4-4266 Eye-Diagram

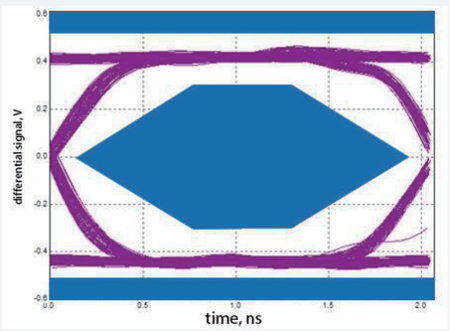
USB PHY SOLUTION

USB Code	Process	Description	H/F/L Speed (Mbit/s)	Power Consumption/ Die Size	Power Supply	Metal Support	Maturity
B14SFP_USB20_PHY	14nm SF+ process	USB2.0 OTG PHY	480/12/1.5	0.05W 0.1872 mm^2	0.8V/1.8V/3.3V	1P9M2TM	Silicon Proven
B28HKCP_USB20_PHY	28nm HKCP process	USB2.0 OTG PHY	480/12/1.5	0.05W 0.3065 mm^2	0.9V/1.8V/3.3V	1P8M2TM	Silicon Proven
B40NLL_USB20_PHY	40nm LL process	USB2.0 OTG PHY	480/12/1.5	0.045W 0.2857 mm^2	1.1V/3.3V	1P8M2TM	Silicon Proven
B55NLL_USB20_PHY	55nm/65nm LL process	USB2.0 OTG PHY	480/12/1.5	0.06W 0.3735 mm^2	1.2V/3.3V	1P7M1TM	Silicon Proven
B55NEF_USB20_PHY	55nm EF	USB2.0 OTG PHY	480/12/1.5	0.06W 0.3735 mm^2	1.2V/3.3V	1P7M1TM	Silicon Proven
B55PFULP_USB11	55nm/65nm LL process	USB1.1 PHY	12/1.5	0.05W 0.0558 mm^2	1.2V/3.3V	1P7M1TM	Silicon Proven
B011_USB20_PHY	0.11umG process	USB2.0 OTG PHY	480/12/1.5	0.057W 0.4280 mm^2	1.2V/3.3V	1P6M	Silicon Proven
B013_USB20_PHY	0.13umG process	USB2.0 OTG PHY	480/12/1.5	0.057W 0.5283 mm^2	1.2V/3.3V	1P6M	Silicon Proven
B013EF_USB20_PHY	0.13um embedded flash	USB2.0 OTG PHY	480/12/1.5	0.057W 0.5655 mm^2	1.5V/3.3V	2P6M	Silicon Proven



USB2.0 PHY Architecture

Brite provides USB2.0 OTG PHY which is a complete mixed-signal IP solution designed to implement OTG connectivity for a System-on-Chip (SoC) design. The USB2.0 OTG PHY supports the USB2.0 480Mbps protocol and data rate, and is backward compatible with the USB 1.1 1.5Mbps and 12Mbps protocol and data rates. This solution can be adapted from 130nm to 14nm process. It has been verified by a number of end products, especially suitable for the current popular internet of things applications.



USB2.0 OTG PHY

FEATURES

- Supports High-speed, Full-Speed and Low-Speed data rates
- Supports Host, Peripherals and OTG application
- Fully Compliant with UTMI + Level 3 Specification
- Supports internal PLL for High-Speed(480MHz) Clock and Data Recovery operation
- Support Built in Self-Test(BIST) for production testing
- Including digital and analog loop back test for HS/FS/LS mode to facilitate testing and debugging
- Integrated Termination Resistors (50Ω, 1.5K, 15K) with auto calibration to meet high accuracy
- Support 8-bit 60MHz and 16-bit 30MHz parallel interface
- Clock and Data Recovery implemented fully by adjustable digital with edge detection to maximizing noise filtering for various applications
- Area and power consumption advantage over competitors

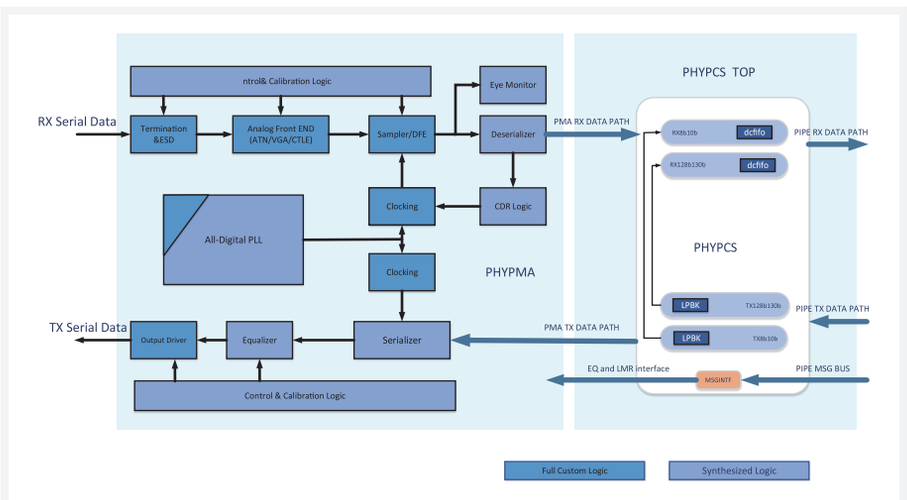
DELIVERABLES

- Datasheet
- User's Manual
- Package/PCB guideline
- SDK (standard design kit) including verilog model, .lib/.db file, .lef file

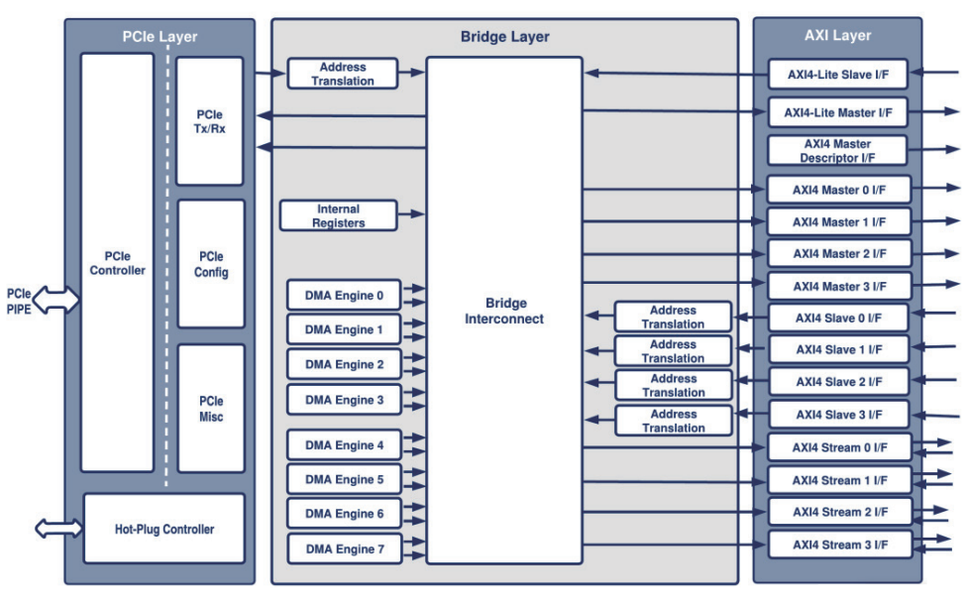
PCIe SYSTEM SOLUTION

Brite 32Gbps PCIe PHY and controller solution provide high efficient interconnection that is optimized for PPA performance. The System can support short-reach or long-reach channels for plenty application scenarios. Besides the high performance of the PHY with its high line rate, low latency operation is a key feature of the PCIe PHY. The PHY supports data rate from 2.5Gbps to 32Gbps to cover PCIe Gen5.0/4.0/3.0/2.0/1.0. The common high-speed LC-PLL clock generation can supply clock up to 8+ lanes depending on jitter requirement, so that flexible macro configuration of e.g. 1x,2x,4x,8x are possible. The top-level block diagram of the PCIe PHY is shown in figure 1.

Brite PCIe controller to AXI architecture is shown in figure 2. It provides a high-performance, easy-to-use interconnect solution between PCI Express and the latest version of the AXI protocol. It inherits the leading architecture and features an AXI user interface with built-in DMA, compliant with the AMBA® AXI3 and AXI4 specifications.



Brite PCIE PHY Block Diagram



PCIE Controller to AXI Architecture

CONTROLLER FEATURES

- x1, x2, x4, x8, x16 PCI Express Core
- Supports link rate of 2.5, 5.0, 8.0, 16.0, and 32.0 GT/s per lane
- 8-bit, 16-bit, 32-bit, 64-bit and 128-bit PIPE interface
- PHY Interface for PCI Express (PIPE), Revision 4.4.1/5.2 compliant
- PCI Express® Base Specification Revision 5.0 v1.0 compliant
- 4 KByte maximum payload size
- 1 Virtual Channel (VC)
- Lane reversal support
- Integrated Clock Domain Crossing (CDC) to support user-selected frequency for the Bridge
- Optional AXI4-Lite Slave interface for Bridge Configuration
- Optional AXI4-Lite Master interface for External Registers Configuration

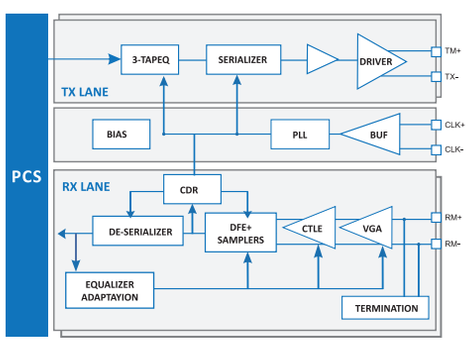
PHY FEATURES

- Metal stack 1P9M, to be specified
- Constant latency of 1.5-word clocks
- Maximum 35dB Insertion loss support
- Flexible macro configurations
- maximum x8 support with a single CMU
- Self-adaption of all major calibration and adaptive processes supported for robust performance
- Software control and override of all auto-adaption processes supported
- Support for both common reference clock and Separate Reference Clock without SSC (SRNS)
- SSC supported
- Max. of +/-300ppm frequency offset for separate reference clock mode
- On-die Eye Monitor for RX performance and TX-to-RX loopback performance
- DIR mode for link EQ training supported (PIPE)
    - RX eye monitor implemented
- Fully compliant with PCIE Express Base 5.0 and 4.0, PCI Express Base 3.1/2.1/1.1 electrical specifications
- PIPE Revision 4.4.1/5.2 compliant
- Different loopback modes: near-end serial, far-end parallel

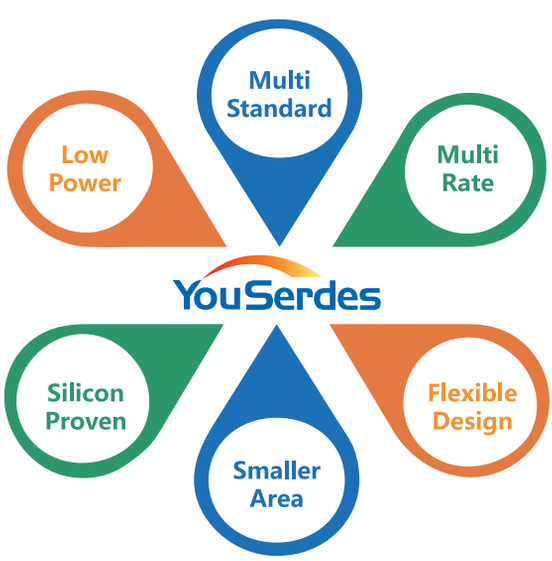
MULTI-RATE SERDES IP SOLUTION

Serdes Code	Process	Power Supply	Speed (bps)	Lane	Metal Support	Power Consumption	Die Size	Maturity
B14SFP_SERDES_32G	14nm SF+	0.8V/1.8V	2.5G~32G	Multiple	1P9M & above	8mW/Gbps per lane +30mW for CMU	2.12 mm^2 GDS size for 8 lane	Paper
B28NHKP_SERDES	28nm HKC+	1V/1.8V	2.5G/5G/8G/16G	Multiple	1P9M & above		6.59mm^2 GDS size for 8 lane	Silicon Proven
B40NLL_SERDES	40nm LL	1.1V/1.8V	12.5G	Multiple	1P8M & above	629mW for 4 lane applications	1.722mm^2 GDS size for 4 lane	Silicon Proven
B40NLL_SERDES	40nm LL	1.1V/1.8V	1.25G-12.5G	Multiple	1P8M & above	12.9mW/Gbps per lane + 7 mW for common block	1.722mm^2 GDS size for 4 lane	Silicon Proven

YouPHY-Serdes provides 1.25-12.5Gbps multi-rate SERDES IP which is designed for smooth integration of Multiple SERDES lanes offering best in class performance, area and power. The programmable PHY supports major standards such as PCIe Gen 1/2/3, USB 3.0 / 3.1, XAUI, SATA Gen 1/2/3, CEI-11G-LR, 10GBase-KX4, JESD204B, SGMII/QSGMII, RAPID I/O, HSSTP (Trace Port), V-By-One, DisplayPort and HMC, based on advanced process as 40nm and 28nm.



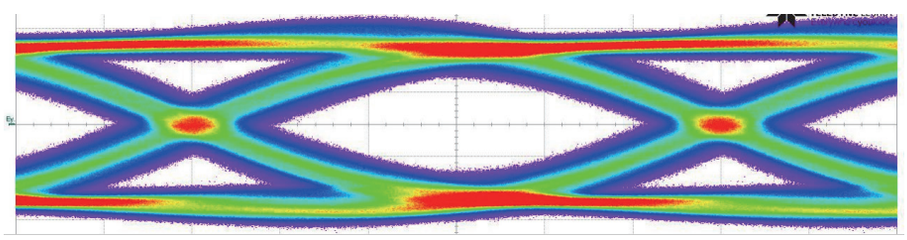
YouPHY-Serdes Subsystem



- Single SERDES Design that meets wide range of Standards, Protocols and Speeds.
- Any combination is possible, e.g. USB-3.0, PCIe Gen-3 and SATA Gen-3 in a single Combo SERDES.
- Internal Low Jitter PLL support the various standards clocking requirements- no need for additional components.
- Flexible Design- Tile Based Design that enable customer to select any number of Tx and Rx Lanes.
- One Time Effort in design, integration, verification and silicon validation.
- Save Chip area as it there is no need to duplicate logic when few standards are required.
- Future Proof Design- design today with your interface roadmap already embedded and verified.

FEATURES

- Unequal number of transmit and receive lanes supported
- Data rate programmable 1.25-12.5 Gbps
- Transmit Driver with programmable output swing 100 – 1100 mVp2p
- Pre/Post cursor Transmit equalization range 0 – 9db/12db with 20mV programmability step
- Adaptive Receiver equalization (CTLE + DFE) to support long-reach channel with insertion loss of 30db at 6GHz
- Embedded low jitter phase-locked-loop (PLL)
- Beacon, Low-Frequency-Periodic-Signaling (LFPS), Auto-negotiation (AN) Signaling supported
- Rich in DFT features (AC-JTAG, Eye-scan, Loop-back, RX Sensitivity BIST, TX level BIST, PLL BIST)
- Stuck-at & TFT scan for digital
- Boundary scan (Extest) for integration with SOC scan compressor
- Tests can be done on low cost digital tester



40LL 12.5Gbps Eye Diagram

Multi- Standards Support

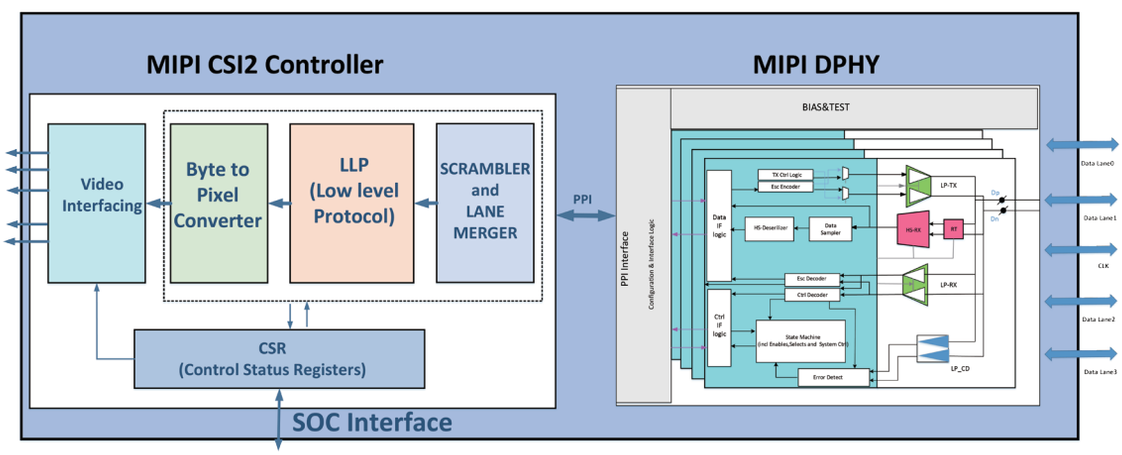
Standards	Data Rate (Gbps)	Organization
PCIe Gen 1/2/3	2.5 / 5 / 8	PCI-SIG
USB 3.0 / 3.1*	5 / 10	USB Forum
XAUI	3.125	IEEE
SATA Gen 1/2/3	1.5 / 3 / 6	SATA
CEI-6G-SR/MR/LR	4.976 – 6.375	OIF Forum
CEI-11G-LR *	9.95 – 11.1	OIF Forum
10GBase-KX4	3.125	IEEE
1000Base-KX	1.25	IEEE
10GBase-KR	10.3125	IEEE
JESD204B	1.25 – 12.5	JEDEC
SGMII/QSGMII	1.25 / 5.0	Cisco
RAPID I/O	9.85	RAPIDIO.ORG
HSSTP (Trace Port)	1.25 – 12.5	ARM
V-By-One	4	Thine Elec.
DisplayPort	8.69	VESA
HMC *	10 / 12.5	HMC Consortium

DELIVERABLES

- Datasheet
- User's Manual
- Package/PCB guideline
- SDK (standard design kit) including verilog model, .lib/.db file, .lef file

CSI2 INTERFACE SOLUTION

Brite provides full solution for the MIPI CSI interface, which receives the data from sensors in PHY layer, and then converts the byte data to pixel after lane data mergence. Data scramble is an optional feature to decrease the EMI effect. A standard PPI interface is implemented for the connection between MIPI PHY and CSI controller. Brite MIPI CSI interface solution supports image applications with varying pixel formats.



Brite MIPI CSI Interface Solution

CONTROLLER FEATURES

- Compliant with MIPI CSI-2 Specification v1.0, v1.1, v1.3, v2.0, v2.1, v3.0
- Compliant with D - PHY Specification v1.1, v1.2, v2.0, v2.1
- Compliant with C - PHY Specification v0.7, v1.2
- Full MIPI CSI-2 RX functionality where either D - PHY / C - PHY can be used
- Supports Multi lane distribution and also lanes can be configured up to 3 lanes for C - PHY and 8 lanes for D - PHY
- Supports Data rate in range 2.5 Gbps
- Supports PPI Interface
- Supports short and long packets
- Supports multilane distribution
- Continuous and non-continuous (gated) D-PHY byte clock support
- Supports Frame and Line Synchronization Packets (Short Packets)
- Supports Data Descrambling in Lanes
- Supports Deskew mechanism for Lane synchronization

- Supports High Speed and Escape Mode (LPDT and ULPS) reception
- Supports the following interleaving methods
  - Data type
  - Virtual channel
- Supports 16 interleaved Virtual channel in D - PHY and 32 in C - PHY
- Support all Protocol Decoding Level errors
- Supports the compression for RAW data types
- Supports Error Detection techniques for active data using Checksum (16 bit)
- Supports Image applications with varying Pixel formats
  - RAW Data Type - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - RAW16, RAW20, RAW24
  - RGB Data Type - RGB444, RGB555, RGB565, RGB888, RGB 666
  - YUV Data Type - YUV422-8bit, YUV422- 10bit, YUV420-8bit
  - YUV420- 10bit, Legacy YUV420-8bit
  - User defined data type - 8 data types
  - Generic 8bit long packet (Null, Blanking, Embedded data)
- Supports Pixel Level /interface with HSYNC, VSYNC, DATA and DATA VALID
- Programmable synchronization and interrupt (error and information) events
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Simple interface allows easy connection to microprocessor/microcontroller devices

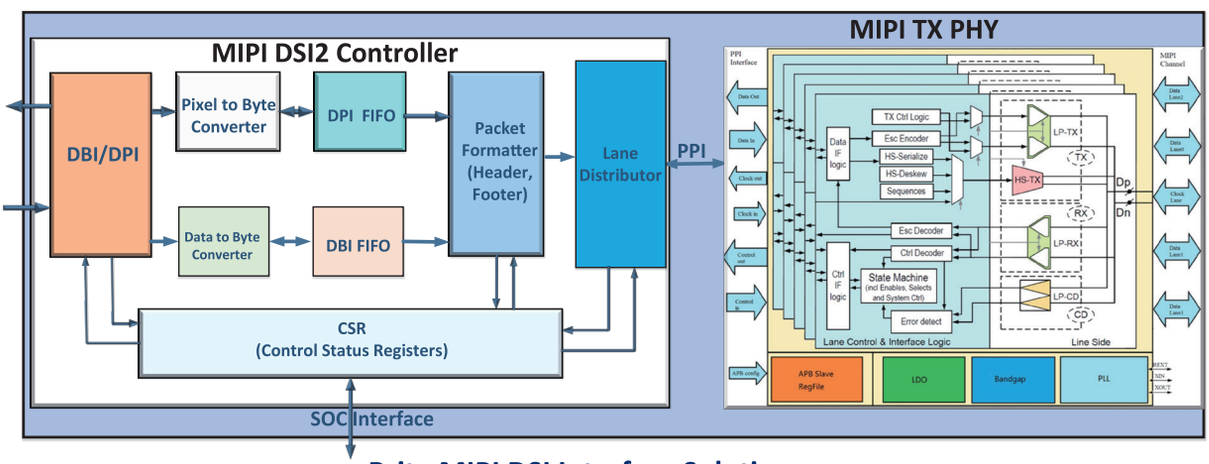
PHY FEATURES

The Brite MIPI DPHY RX integrates 1 clock lane and up to 4 Data lanes, which is compatible with the D-PHY V1.2specification. The high speed receiver supports 80Mbps up to 2.5Gbps data rate, low-power receiver and transmitter both support data transmission around 10Mbps. As the same as TX, the interface is a standard MIPI D-PHY PPI interface that can be easily connected to a standard CSI controller.
More features can be provided by the B14SFP_MIPI_DPHY RX IP:

- On-die automatic termination calibration to PVT.
- Automatic termination control for HS and LP modes.
- MIPI-HS/MIPI-LP modes Support.
- BIST
- PRBS Checker

DSI2 INTERFACE SOLUTION

Brite provides a complete MIPI DSI2 solution, which is compliant with MIPI DSI-2 specification. It supports 1 to 4 lane configuration and different data formats, which can adapt to diverse application scenarios. The DPHY can support crystal or SOC clock input as reference clock, and the data lane sequence can be freely swapped. The interface between controller and PHY is a standard PPI interface.



Brite MIPI DSI Interface Solution

CONTROLLER FEATURES

- Compliant with MIPI DSI-2 Specification v1.3
- Compliant with Display Serial Interface (DPI -2) v2.0
- Supports fully MIPI DSI2 Transmitter functionality
- Compliant with Display Bus Interface (DBI) v2.0
- Compliant with Display Command Set (DCS) v1.3
- Compliant with D - PHY specification v1.1, v1.2, v2.0, v2.1
- Compliant with C – PHY specification v1.2
- Full MIPI DSI-2 Receiver functionality supporting CPHY and DPHY
- Supports all types of short and long packets
- Supports 1 to 4 lane configuration and 3 trios
- Supports internal data width of maximum up to 128 bits
- Supports PPI interface with 8/16/32 bit
- Supports all virtual channel identifier

- Supports both video and command modes
- Supports Multiple packets per transmission
- Supports Error Detection techniques for active data using Check sum (16 bit)
- Interrupt support for indicating internal status and error information
- Supports sync event payloads and Data Interleaving
- Programmable display resolutions
- Supports for dual MIPI DSI use case with VESA display stream compression (DSC)
- Supports generic read / write over DBI Interface
- Supports burst and non-burst mode transfer over DPI Interface
- Supports all BTA (Bi directional Turn around) with contention and fault recovery
- Supports Bi-directional communication and escape mode
- Supports EOT Enable/ Disable Mechanism
- Supports Link Merging Function
- Supports both High speed and Low power packet reception
- Multiple peripheral support capability with configurable virtual channels Supports for ultra- low power mode
- Supports following formats
    - YCbCr Data type
    - RGB Data type
    - YUV Data type
    - RAW Data type
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Simple interface allows easy connection to microprocessor/microcontroller devices

PHY FEATURES

The Brite MIPI DPHY TX integrates 1 clock lane and up to 4 Data Lanes compatible high-speed receiver that support 80Mbps up to 2.5Gbps Data rate, low-power receiver and transmitter that supports data rate around 10Mbps. This IP supports D-PHY v1.2specification. The interface is a standard MIPI D-PHY PPI interface that can be easily connected to a standard DSI controller.

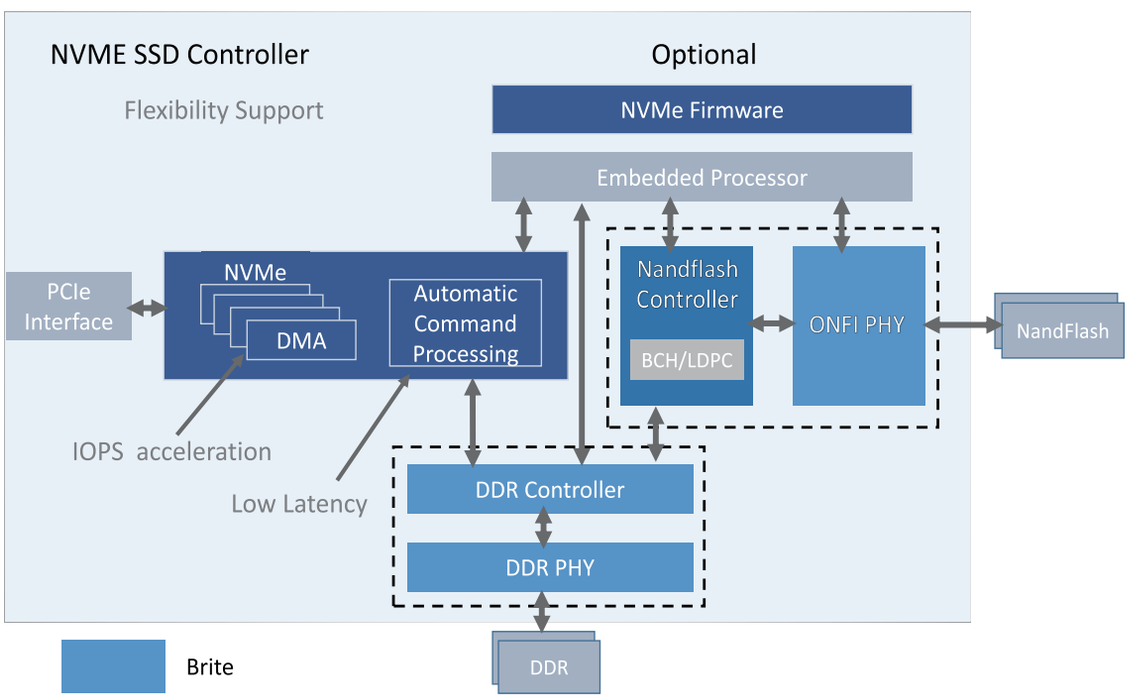
As well, the Brite MIPI DPHY TX consists of many key components which provides a variety of functionality:

- On-die automatic TX termination calibration.
- SCAN and BIST modes.
- Flexible input clock reference
- Lane Swap supported
- Internal reference clock or external crystal oscillator support

BRITE NAND PHY

PHY FEATURES

- ONFI 1/2/3/4/5 compliant
- SLC/MLC/TLC support
- SDR (Asynchronous) mode 0 to 5
- NV-DDR (Source Synchronous) mode 0 to 5
- NV-DDR2 mode 0 to 10
- NV-DDR3 mode 0 to 15
- NV-LPDDR4 mode 0 to 19
- Toggle/Toggle2 mode
- Maximum 2400Mbps (PHY_CLK = 1200Mhz)
- X8/X16 support
- 1.2V/1.8V/3.3V support
- All-Digital-DLL
- APB register interface (Asynchronous to PHY_CLK)
- SMIC 14SFP, 40LL



HIGH SPEED I/O SOLUTION

DDR IO

Brite DDR (Double Data Rate SDRAM) IO libraries cover wide range of DDR standards, from DDR2 to DDR5 and LPDDR2 to LPDDR4 with the data rate from 200Mbps to 4800Mbps, based on SMIC 65nm LL process to 14nm FinFET process respectively. Brite provides competitive features of DDR IO, including OCD, ODT, DCC and VREF calibration and TX de-emphasis options, to achieve high speed performance, low jitter, low power and compact cell size.

DDR IO Code	Process	DDR2 (Mbps)	DDR3 (Mbps)	DDR4 (Mbps)	DDR5 (Mbps)	LPDDR2 (Mbps)	LPDDR3 (Mbps)	LPDDR4 (Mbps)	Maturity
B14SFP _DDRIO_DDR45	14nm SF+	--	--	3200	4800	--	--	--	Paper
B14SFP_DDRIO_DDR4LPDDR34	14nm SF+	--	--	3200	--	--	2133	4266	Silicon Proven
B14SFP_DDRIO_DDR34LPDDR34	14nm SF+	--	2133	3200	--	--	2133	3200	Silicon Proven
B28HKCP_DDRIO_D34LP234	28nm HKC+	--	2133	2666	--	--	2133	2666	Silicon Proven
B40NLL_DDRIO_D34LP23	40nm LL	--	1866	1866	--	1066	1866	--	Silicon Proven
B40NLL_DDRIO_COMBO	40nm LL	1066	1333	--	--	1066	1066	--	Silicon Proven
B55NLL_DDRIO_D4	55nm LL	--	--	1866	--	--	--	--	Silicon Proven
B55NLL_DDRIO_COMBO	55nm/65nm LL	1066	1066	--	--	1066	1066	--	Silicon Proven

ONFI IO

ONFI (Open NAND Flash Interface) IO is applied for NAND flash memory interface. Brite ONFI IO libraries are compliant to ONFI 4.1/4.0/3.2 standards with ODT (On-Die Termination) and impedance calibration functions, based on SMIC 14nm FinFET and 40nm LL process.

ONFI IO Code	Process	SDR (Mbps)	NV_DDR (Mbps)	NV_DDR2 (Mbps)	NV_DDR3 (Mbps)	NV_DDR4 (Mbps)	Maturity
B14SFP_ONFI5_IO	14nm SF+	--	200	800	1600	2400	Paper
B14SFP_ONFI4_IO	14nm SF+	--	200	800	1600	--	Silicon Proven
B40NLL_ONFI4_IO	40nm LL	100	200	800	800	--	Silicon Proven

LVDS IO

LVDS IO Code	Process	2.5V Mode (Mbps)	1.8V Mode (Mbps)	Maturity
B14SFP_LVDS_IO	14nm SF+	--	2000	Paper
B28NHKP_LVDS	28nm HKC+	--	1600	Silicon Proven
B40NLL_LVDS	40nm LL	1600	1600	Silicon Proven

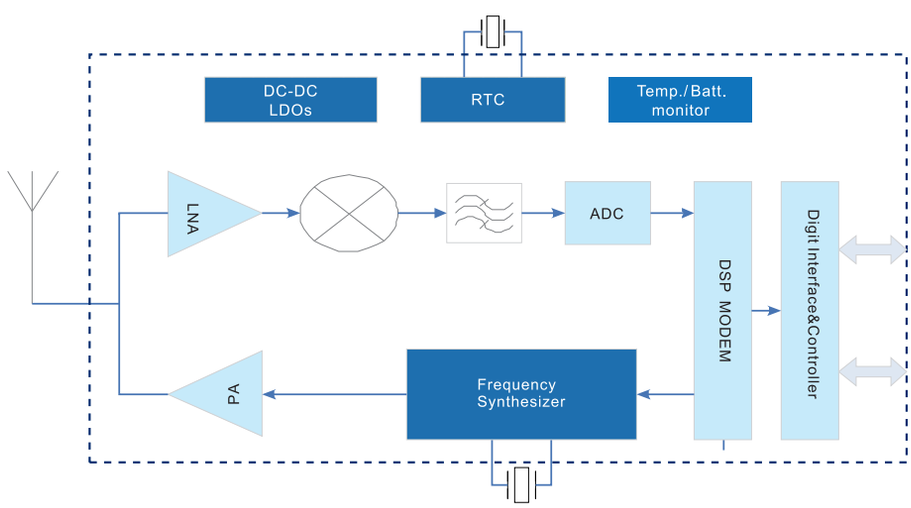
LVDS (Low Voltage Differential Signaling) IO can be applied for various die-to-die interface communication. Brite LVDS IO libraries can support data rate up to 1600Mbps with 2.5V and 1.8V power, based on SMIC 14nm FinFET, 28nm HK and 40nm LL process.

YouRF-BLE

BLUETOOTH LOW ENERGY IP

IP Code	Process	Supported Mode	Sensitivity Power (dBm)		Power Consumption (mW)		Input Voltage (V)	Metal Support	Maturity
			RX	TX	RX	TX			
B55NLL_BLE_PMU	55nm LL	Active mode, Idle mode Standby mode Shutdown mode	<-92dBm	--	<10mW	<12mW	1.8~4.3V	1P6M	Paper

Brite provides a complete Bluetooth Low Energy (BLE) analog PHY. The RF is a high performance 2.4GHz ISM band wireless transceiver. It integrates high sensitivity receivers, 5G PLL and high efficiency power amplifier, which can support 1Mbps GFSK modulation and demodulation, and can be combined with the Bluetooth smart baseband and controller to form a complete Bluetooth Smart solution.



Block Diagram

FEATURES

- Leading technology of SMIC 55nm LL_RF process.
- Single supply voltage: 1.8 to 4.3V
- Operating junction temperature: -40°C to 85°.
- RF output power up to +4dBm
- Receiver sensitivity: <-92dBm
- Build-in on-chip Buck DC/DC converter and LDOs
- Low power consumption: RX<10mW; TX<12mW@0dBm
- Flexible, Rectangular PHY layout hardened to match IO pad frame.

DELIVERABLES

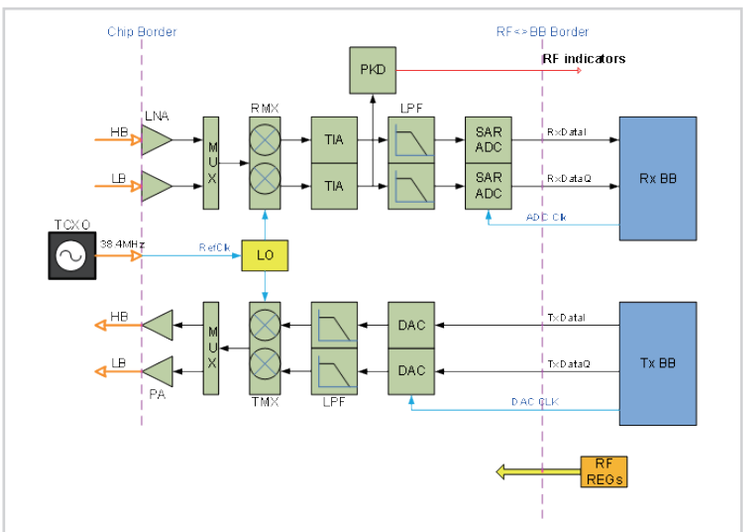
- Datasheet.
- Encrypted Verilog simulation model (ncverilog/vcs)
- .db, .lib, .vg, .lef, .sdf
- Timing report.

NB-IOT

The B40NLL_NBIOT_TRX is a sub-1GHz (699MHz-960MHz) fully integrated transceiver specially designed for Narrow-band IOT applications. The device is comprised of RF frontend, Frac-N frequency synthesizer, LO chains, and analog baseband blocks. The receive path (RX) has high dynamic range and sensitivity. A zero-IF TX generates low EVM signals to drive the external power amplifier. The fully integrated Frac-N frequency synthesizer generates required low-phase-noise LO signals for TX and RX mixers.

B40NLL_NBIOT_TRX is developed with SMIC 40nm Low Leakage RF 1P7M process.

The supply voltage ranges from 2.8V to 3.6V. A 38.4MHz temperature controlled oscillator (TCXO) is used as a reference clock.

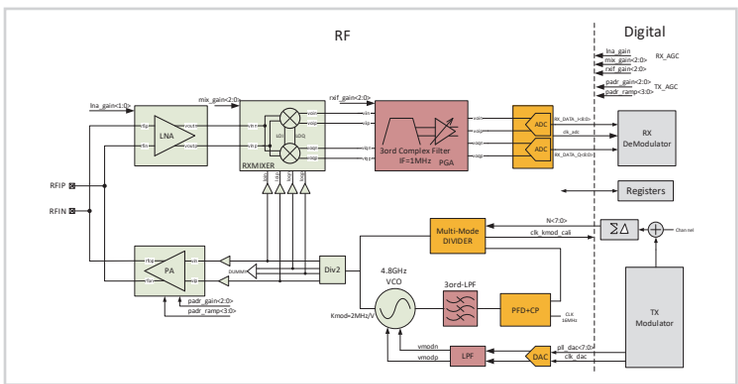


NB-IoT Solution

PROPRIETARY 2.4G

The transceiver chip will use external 1.9V-3.6V as the input power and internal LDOs to generate the internal supply voltages.

The receiver has a low-IF architecture and uses off-chip single-ended to differential signal conversion (via a matching network). The signal is received from the antenna and then is amplified by an LNA before being sent to RXMIXER. The in-phase and quadrature-phase outputs of the RXMIXER are then passed on to complex filters for channel selection. The output of the filters are passed on to baseband PGA and then sent to the 9bit ADCs. The final down conversion to baseband and actual image rejection are performed in the digital domain.



Proprietary 2.4G

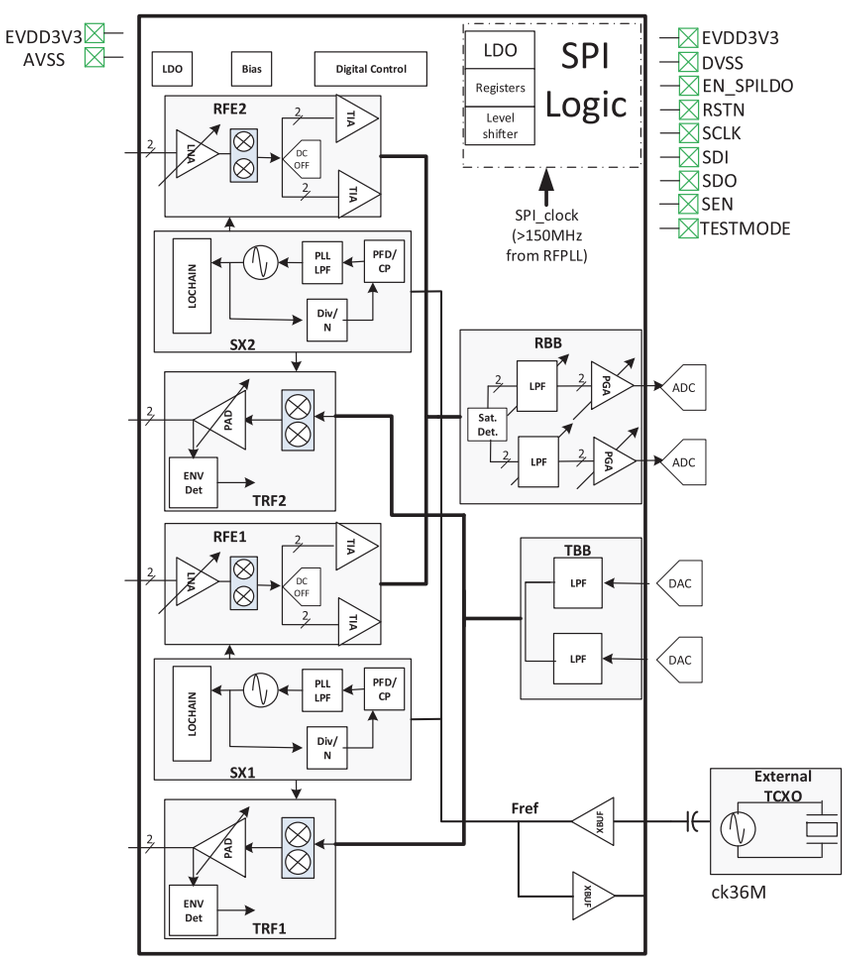
TX has a two-point closed-loop modulation architecture. The local oscillator contains a fractional-N PLL which is used to generate the phase modulated signal. The output of the RFPLL is fed into the PA driver through a LO buffer to isolate the PA and the LO.

TRANSCEIVER 802.15.4G

The RF Transceiver (B130RF15P4G)is a dual band (sub-1GHz and 2.4GHz band) fully integrated transceiver specially designed for smart metering and IEEE 802.15.4g related applications.

The RF Transceiver provides high performance, low-cost, generic RF front-end that allows several constant and non-constant envelope modulation schemes to be handled, such as the MR-FSK, MR-OFDM and MR-O-QPSK PHYs of the IEEE 802.15.4g standard for Smart UtilityNetworks (SUN) and Smart grid applications in the 850 - 928 MHz and 2.4GHz license-exempt frequency bands.

The supply voltage ranges from 3.0V to 3.6V. A 36MHz temperature-controlled oscillator (TCXO) or a crystal oscillator (XTAL) is used as a reference clock.



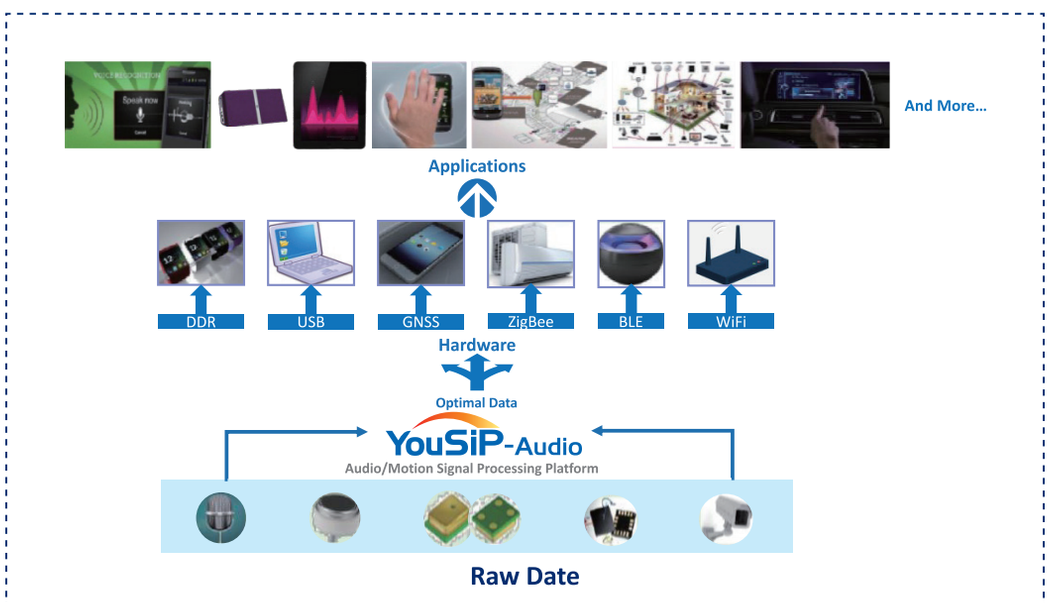
RF Transceiver IP

YouSiP-Audio

Audio DSP PLATFORM

Audio/Voice DSP reference design platform is developed based on the dual Tensilica DSP cores.

- The platform provides designers with a powerful means to add “smart and connected” capabilities to these devices, including always-on sensing, local processing, and intelligence connectivity.
- The platform provides real-time power measurement that allows developers to reduce power consumption of system by optimizing their DSP software effectively.
- The platform provides a complete development and demo system integrating DSP and multiple peripherals & interfaces IP, and supports diverse wireless technologies including Bluetooth Smart and Smart Ready, Wi-Fi, ZigBee and GNSS.
- The platform can be adopted on mobile, wearable devices, wireless speaker, home entertainment, smart home, surveilance, automotives and so on.



YouSiP-Audio ADVANCED APPLICATION SUPPORT

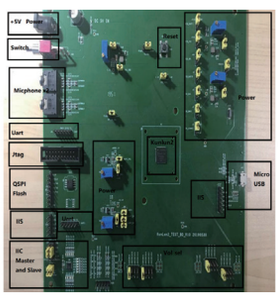
YouSiP-Audio develops a total hardware solution to collect the raw audio, voice, motion, ultrasonic, and image signal data, and then passes them to the host equipment.

- Developers can be easier to porting their software to verify different applications that can help customer to win the emerging market as voice control, sports management, gesture detector, indoor navigation, smart home, automotive infotainment and so on efficiently.
- The first amazing function achieved by YouSiP-Audio is voice command. You can control this demo board to play and shuffle music by voice directly. It is a dreamy image that you can talk and interact with the equipment around. And it can be adopted more in the smart home applications.

YouSiP-Audio

Application and Functions		Target Markets					
							
		Mobile & Wearable	Wireless Speakers	Home Entertainment	Smart Home	Surveillance	Automotive
Voice capture	Beam forming (multi-microphone); Noise reduction; Echo canceller; Vocoders	√	√	√ Far-field	√ Far-field	√ Far-field	√
Always-on voice activation	Voice trigger; Voice command;Speaker verification;Soundsensing	√	√	√	√	√	√
Always-on sensor-fusion	Motion sensors processing; Ultrasonic gestures; Face detection	√	√ Ultrasonic	√ Face detection	√ Face detection	√ Face detection	√
Audio processing	High-endaudio codecs; Post processing; Audio encode	√ Android offloading	√	√ Multi-channel	√ Multi-channel	√	√ Multi-channel
Wireless connectivity	BT dual mode; BLE;WiFi	√	√	√	√	√	√

YouSiP-Audio SOLUTION AND EVB BOARD



- Strong functions as voice capture, always-on voice activation, always-on sensor-fusion, audio processing and wireless connectivity can be supported by YouSiP-Audio.
- It can achieve up to 400MHz speed, and provides real-time power measurement to improve power consumption of system by DSP software optimizing effectively. To provide a complete development and demo system, it contains TDM, DMA, I2C, I2S, ICU, Timers, GPIO, and especially Tensilica DSP. Multiple peripherals and interfaces, such as digital microphones, sensor I2C I/F, AD audio codec
- input/output, USB, UART, PCIe and Ethernet, can enable customer to configure FPGA, GPIOs, DDR memory, SD card and LCD display easily, and shorten time-to-market of product.

YouSiP-Audio TENSILICA DSP PERFORMANCE

- Strong performance: supports up to six microphone pickup, strong anti-interference ability, quick response, high wake-up rate
- Low power consumption: milliwatt idle power consumption, hundred milliwatt full speed working power consumption, suitable for portable devices
- Offline recognition: supports full offline recognition, and can recognize more than 100 instructions offline
- Rapid deployment: built-in algorithm, can customize keywords and quickly deploy to various devices
- Flexible application: supports multiple layout schemes, and meet the needs of various IOT products

YouSiP-Audio TENSILICA DSP SPECIFICATIONS

- HiFi4 audio engine
- Frequency up to 400MHz
- 32KB Dcache and 16KB Icache
- 32KB IRAM and 48KB DRAM
- Customized TIE instruction for application related voice processing algorithm
- AXI master and slave port for high bandwidth requirement with data width of 64bit
- Support internal DMA with AXI-64bit interface
- 32 configurable interrupts
- JTAG debug port

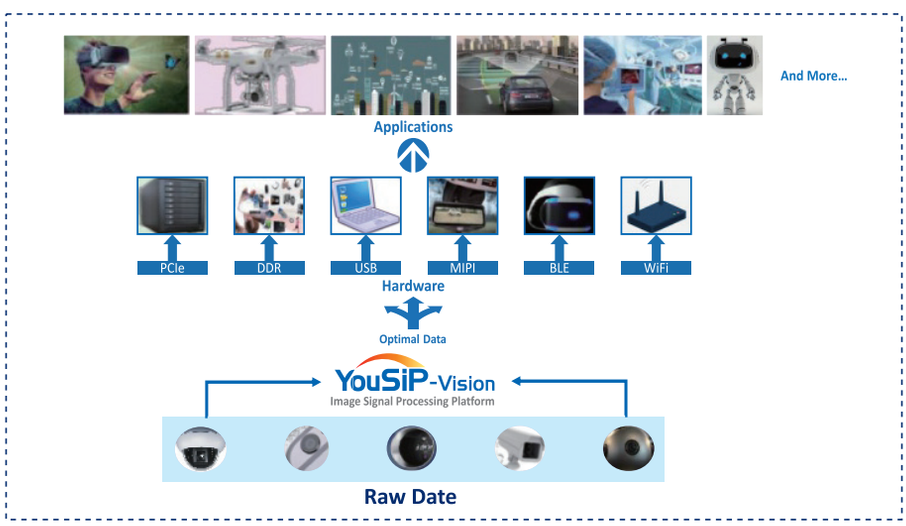
YouSiP-Vision

Vision ISP PLATFORM

It is an image signal processer (ISP) platform integrated some high speed interface IPs, such as MIPI, PCIe, LPDDR3, and USB, which is developed based on SMIC 40nm and 14nm process.

It supports 3D vision (including real-time 3D depth map generation and point cloud processing for 3D scanning), computational photography algorithms (including refocus, background replacement, zoom, super-resolution, image stabilization, HDR, noise reduction, and improved low-light capabilities), and visual perception (including deep learning, object detection, recognition & tracking, context aware, augmented reality(AR) and others).

This platform targets any camera-enabled devices such as smartphones, tablets, automotive safety (ADAS) and infotainment, robotics, security and surveillance, augmented reality (AR) and virtual reality (VR), and drones.



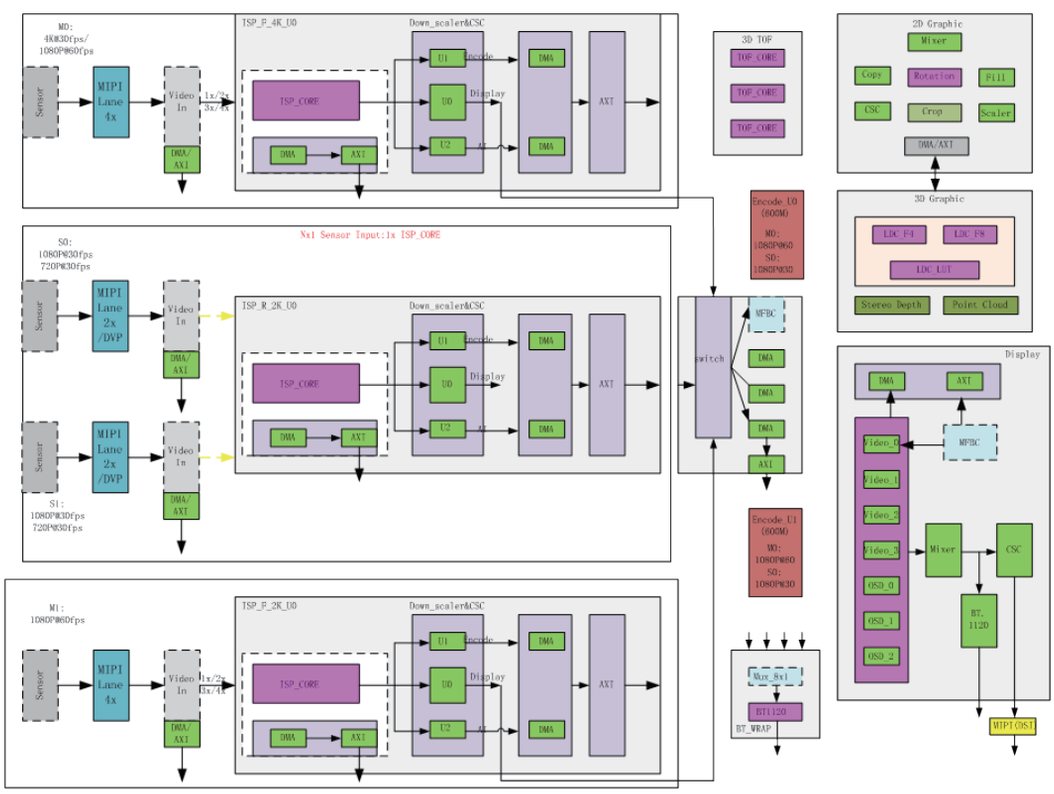
APPLICATION SCENARIOS

- Traditional Surveillance(IPC)
- Smart Transportation (ITS)
- Automobile(ADAS)
- Unmanned Aerial Vehicle(UAV)
- Industrial Detection
- Artificial Intelligence(AI)
- AI plus Surveillance
- Medical
- 3D Depth Industry(TOF)



CORE COMPETENCE

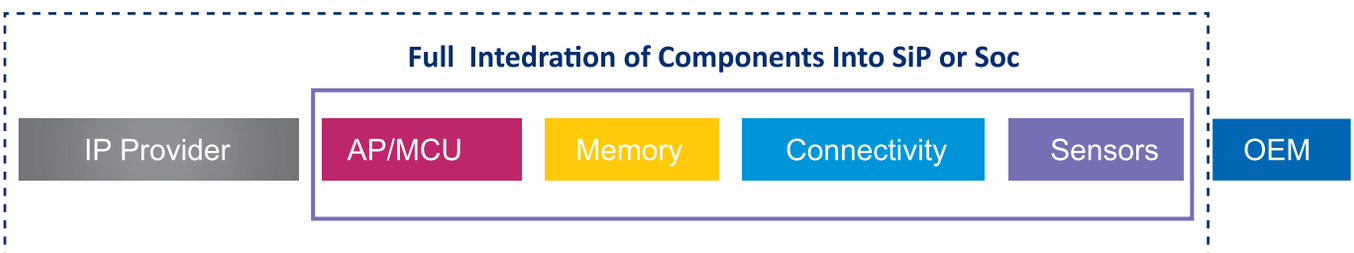
- Deeply Understanding of Application of Various Industries
  - M/P in various industries
  - Including, but not limited to surveillance, UAV, ITS, industry detection, AI, and medical
- Wide Range Product Line and Features
  - Both 2D/3D ISP support, other video IP is optional
  - Full features are supported, such as latest Single/Multi Frame WDR, and RGBIR
- Cost-Effective Solution
  - Optimized implement architecture and pipeline
  - Best resource share and minimal silicon area, less than one third of competitors
  - Easy Integration and shorter time-to-market
- Flexible Configuration and Support Strategy
  - Flexible configuration to meet different application
  - Timely and high quality support team to reduce resource effort of SoC customers



YouSiP-IoT

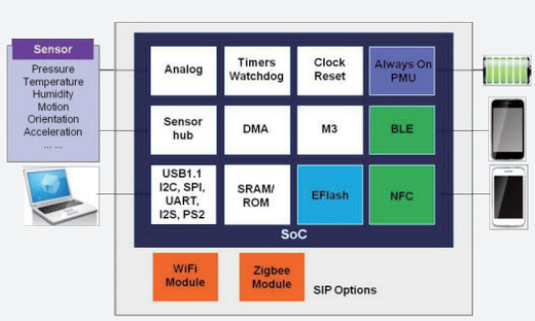
IoT PLATFORM SOLUTION

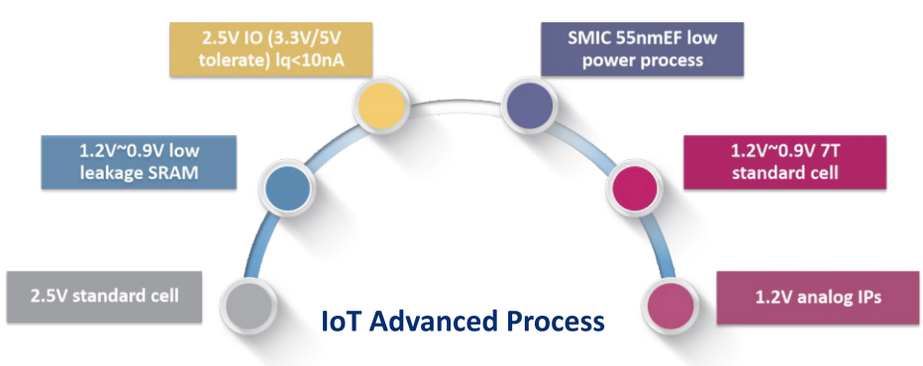
YouSiP-IoT is a comprehensive platform solution designed for emerging application as IoT based on SMIC 55nm low leakage (LL) and 130nm Mixed signal Low leackage(LL) process which can provide embedded non-volital flash memory as well. This solution integrates ARM Cortex Mx series MCU and CEVA TeakLite or MM series DSP, involves WiFi, Bluetooth/BLE interfaces, which can connect to a series of different sensors. YouSiP-IoT platform can assist customer to reduce the processing delay time, enhance the data security, improve the data rate and reduce power consumption of their SoC design, which is adopted in battary power supply environment as smart home, IoT and wearable devices with excellent low power managment.



IoT HARDWARE PLATFORM SOLUTION

- Flexible computing power
  - M0, M0+, M3, M4,
- Internal resource
  - SRAM
  - ROM
- DMA engine
- Embedded flash
- Rich IO interfaces
- Embedded PMU
- Integrated RF solutions
  - Complete BLE + NFC
- SIP MEMS/RF
  - MEMS, WiFi, Zigbee, etc
- Easy to customize





LOW POWER DESIGN FOR IoT

Low power process and library	Embedded PMU	Dynamic clock voltage scaling	Multiple Power Islands
Ultra low leakage and flexible Always Domain	Power States	Clock gating	Ultra low power design flow

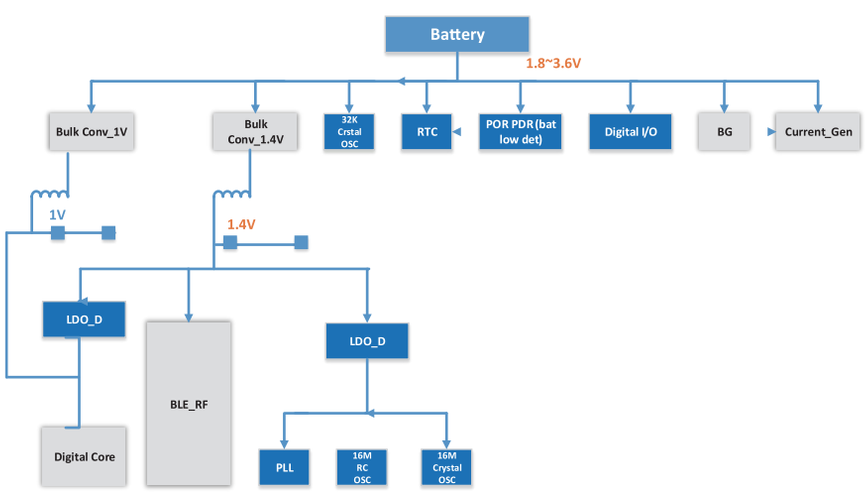
POWER MANAGEMENT UNIT (PMU) FOR IoT

General Description

Power-consumption will affect the IoT's functionality, and power management has become one of the most important and differentiating feature in the low power application such as wearable. Many devices have multiple internal voltages (e.g., 5 V, 3.3 V, 1.8 V, etc.) and sources of external power to charge their batteries including USB. Brite's Power Management Unit (PMU) provides high efficiency power conversion that minimizes energy loss, and is used in battery-powered devices, smart appliances, healthcare, home automation, consumer electronics, industrial automation.

Brite's PMU for complete low power management solution

- Low power DC-DC bulk
- Low power charge pump
- Low power LDO



Brite's PMU example
(IoT Power Supply Domain Diagram for SMIC55nm)

Power Supply, 1.8 (0.9) ~ 5.5V

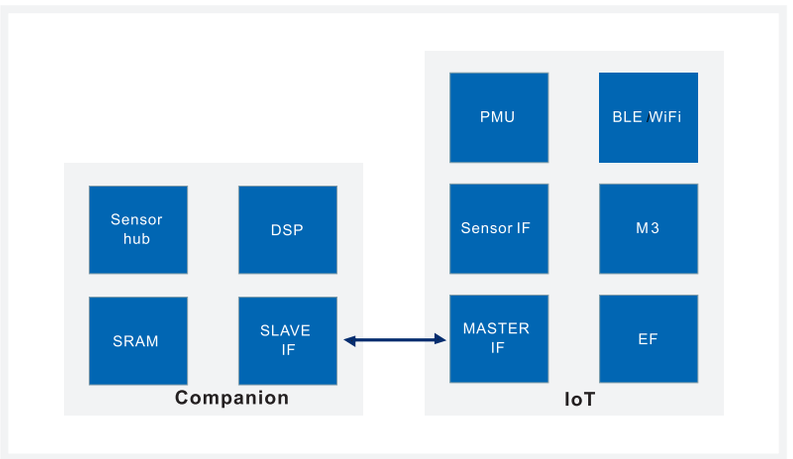
- Chargeable Li-ion battery 3 ~ 4.3V
- 5V charge solution: external charge controller
- Lithium coin-cell or 2 Alkaline batteries 1.8 ~ 3V
- USB Vbus 4.5 ~ 5.5V

IoT COMPANION CHIP SOLUTION

To differentiate customer's applications by voice recognition, finger print, gesture detection etc.

Sensor Hub/Fusion

- Analog
  - 4 Analog IO
  - Optional PGA
  - Programmable threshold
- Digital
  - Up to 6 triggers

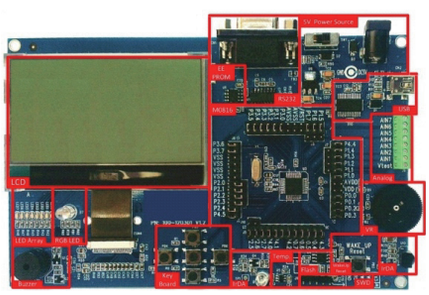


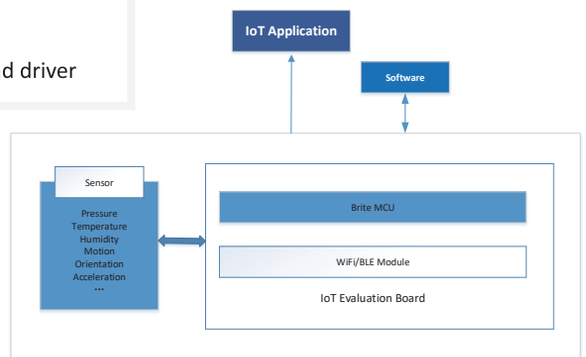
DSP-CEVA TeakLite410 core

- High-Performance, Low-Power Audio/ Voice/ Sensing and Wireless Communication Apps
- Native 32-bit, variable 10-stage pipeline, fixed-point DSP architecture
- More powerful TL411

IoT DEVELOPMENT TOOL AND ENVIRONMENT

- Evaluation Board with Brite MCU + WiFi/BLE module
- EVB is provided to customers for early-stage system development
  - All functions with ready peripheral
  - Open example codes and driver





YouSiP-IoT EVB

SECURITY SOLUTIONS FOR IoT

Key Security Use Cases

- Authentication and authorization
- Secure control interface
- Secure information going in (code, data)
- Secure data going out (telemetry)
- Support protocol security requirements (HK. AJ, others)

Low Power Design	Security Solutions	BLE SDK Features	Wireless Connectivity
Low power process and library Embedded PMU Dynamic clock voltage scaling Multiple Power Islands Ultra low leakage and flexible Always Domain Power States Clock gating Ultra low power design flow	Key Security Use Cases: •Authentication and authorization •Secure control interface •Secure information going in (code, data) •Secure data going out (telemetry) •Support protocol security requirements (HK. AJ, others)	•Quick start the product without pay much effort on the BLE stack & chip BSP. •Provide complete SDK	**Embedded BLE** BLE4.2,Complete RF + Modem + Link Layer **RF features** •RF output power up to +2dBm •Receiver sensitivity: < 92dBm •Low power consumption: RX<10mW; TX<12mW@0dBm •Build-in on-chip Buck-Boost DC/DC converter and LDOs **SIP through UART / I2C** BLE, WIFI,Zigbee, NFC, ……

HW Footprint Considerations

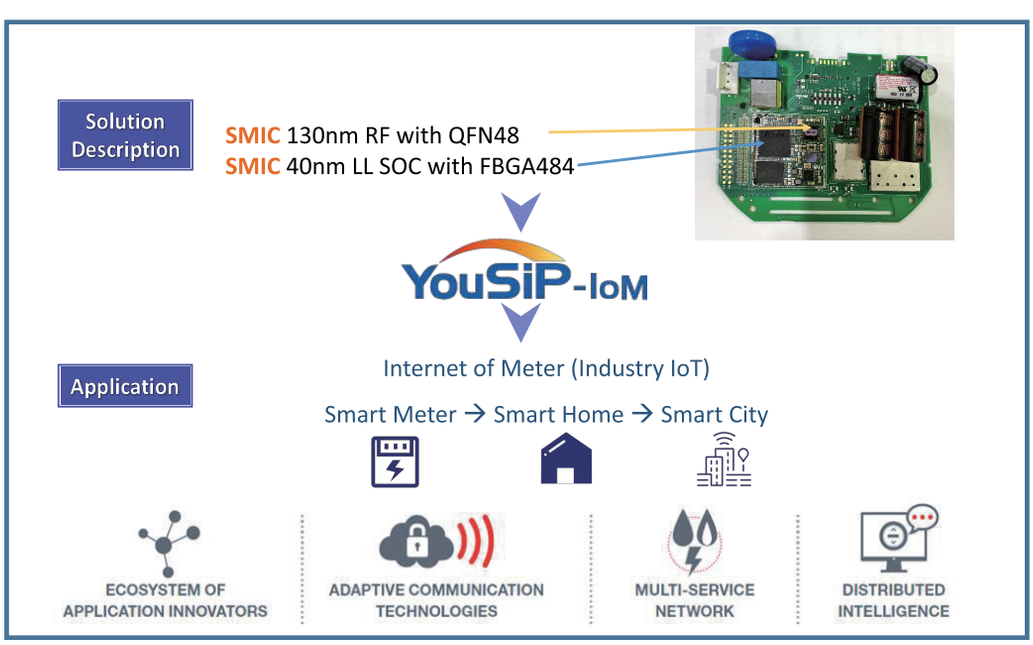
- Secure Boot (include SW RSA, Hash)
- AES
- HASH
- TRNG
- PKA

INTERNET OF METERS PLATFORM

YouSiP-IoM is an innovative interconnection SoC solution for smart meters developed by Brite. This platform bases on ARM Cortex A7 and Cadence Tensilica LX6 DSP architecture which can provide strong core computing and communication capability. Multiply transmission interface IPs are integrated to support industrial level wire and wireless connection as PLC, IEEE 802.15.4g and WiFi which can bring intelligent and connection to smart water, electricity and gas meters. Abundant peripheral interface containing NAND Flash, LPDDR1/2, SD/MMC, USB 2.0 OTG, UART, SPI, I2C and RTC enable designer to extend sensing function and smart measuring technology and adapt product on various emerging applications and systems. Low power and high security design can assist customer to shorten time-to-market of industrial meter products. Silicon proven YouSiP-IoM platform is an amazing transmission SoC solution to help customer to achieve meter smart, home smart and city smart.

FEATURES

- Distributed intelligence
  - Location awareness for every meter
  - Multi-protocol support for complex network environment
  - Super processing capability for accuracy measurement
- Adaptive communication technology
  - Self-select optimal communication mode for operating
  - circumstances
  - Flexible floorplan based on various connect mode
- Multi-service network
  - Smart interconnect between meters
- Ecosystem of smart application
  - Smart interconnect between home and city
- Low power design for battery application (<1W worst case)



YouSiP-AP

AP PLATFORM

YouSiP-AP provides an ARM Cortex-A series core architecture based on SoC platform prototype which has been verified on SMIC 28nm and 40nm process. Its complete development tool including ISP/ICP tools, development boards, reference code and programmer and peripheral IPs can be offered to customer, enabling customer to achieve SoC product with shorter time to market and higher one time delivery rate and assisting them win the emerging market opportunities in the field of industrial control, home appliance, security, toys, mobile devices, etc.

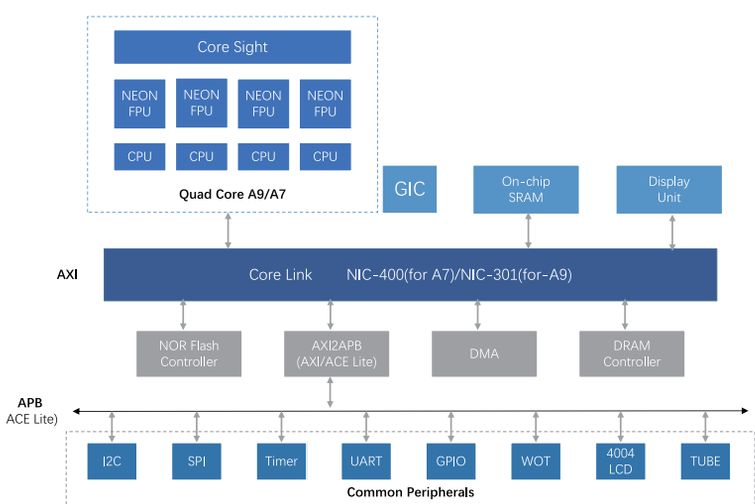
Cortex-A9/A7/A5 processors provide design flexibility by extending the required peak performance points and scalability, and delivering the desired power efficiency, and silicon cost while maintaining full software compatibility.

Core	Cortex-A5	Cortex-A7	Cortex-A9
Architecture	ARMv7+MP	ARMv7+MP+LPAE	ARMv7+MP
Interrupt Controller	GIC-390	GIC-400	GIC-390
	(Integrated GIC for MPC)		(Integrated GIC for MPC)
L2 Cache Controller	L2C-310	Integrated L2	L2C-310

The Cortex-A9 processor is available as 1-4 core, multi-core processors with the additional advantages of cache coherence, integrated peripherals and advanced bus interface options. Brite's dual-core hard macro is implemented in SMIC 40LL that can achieve 1.3GHz at 25oC, TT. This macro provides a low-risk, and accelerated path to deliver the low power solution for various high performance markets.

The Cortex-A7 processor is similar in power and area to the ultra energy-efficient Cortex-A5 processor, but a 15~20% better performance. The advanced features include large physical address extensions (LPAE), hardware virtualization support, and AMBA4 ACE (AMBA Coherency Extension). This small and power efficient CPU is ideal for Brite's customers who want the latest low-cost smart-phone and tablet applications as a standalone processor.

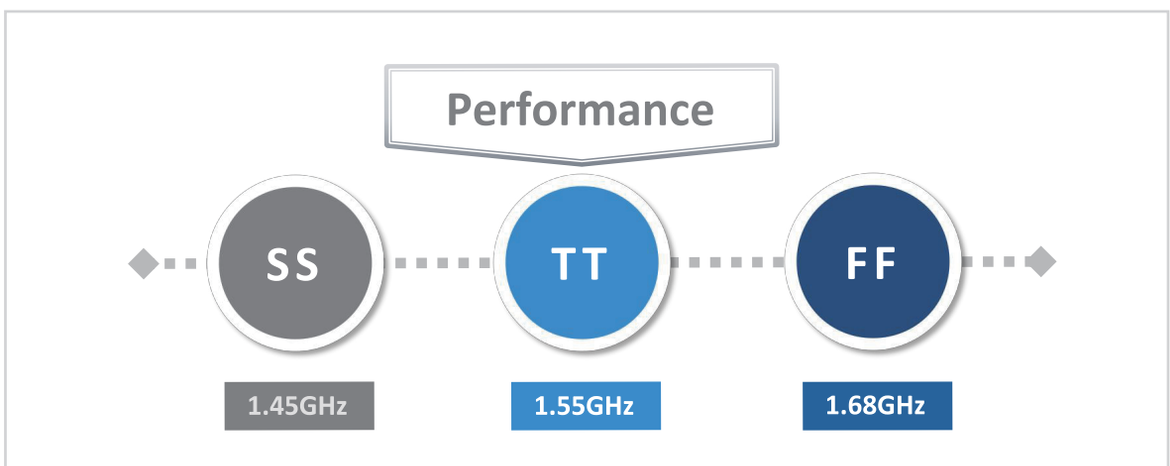
The Cortex-A5 processor is the smallest, lowest power multicore processor capable of delivering the Internet to the widest possible range of devices: from ultra low cost handsets, feature phones and smart mobile devices, to pervasive low power embedded solutions with a high performance and rich UI requirements, consumer and industrial devices. The Cortex-A5 processor is fully application compatible with the Cortex-A9 with 1/3 the power and area, enabling Brite's customers immediate access to an established developer and software ecosystem including Android, Adobe Flash, Java Platform Standard Edition (Java SE), JavaFX, Linux, Microsoft Windows Embedded, Symbian and Ubuntu.



Virtual SoC Configuration for Cortex-A9/A7

YouSiP-AP 40nm HIGH PERFORMANCE CPU CORE

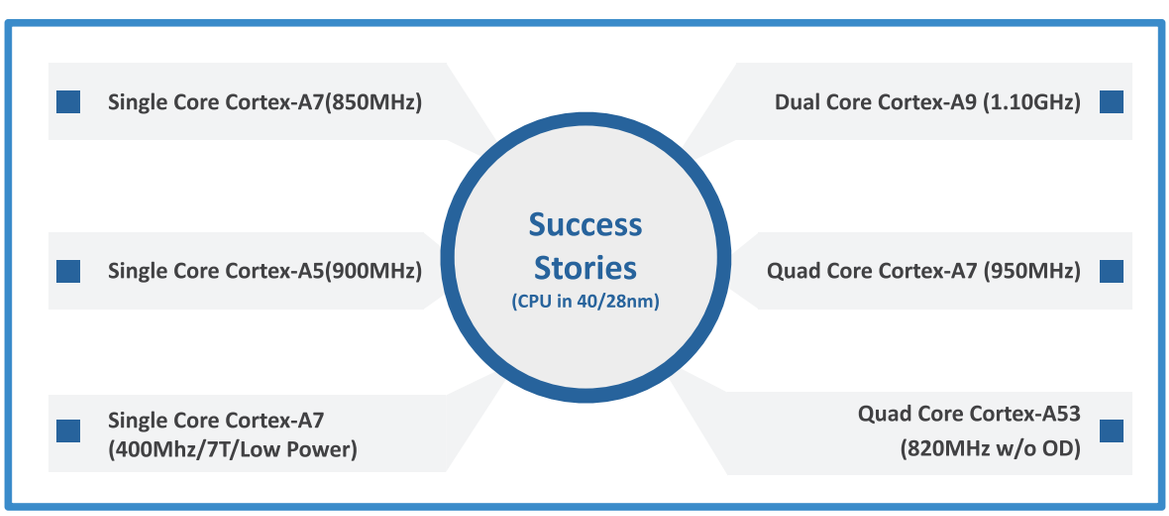
- With accurate SMIC 40LL models, silicon performance meets simulation
- Leakage current less than 40mA for TT wafer with 1.2V in 25°C
- Several types of FPGA verification systems are completed for customers' reference
- Early stage software and function development can be achieved with these FPGA verification systems



Silicon Data, in 25oC, 1.2V with ULVT

SUCCESS STORIES FROM BRITE

- Brite completes 20+ ARM Cortex-embedded projects.
- First cut work from implementation point of view via strong technical capability.



Your Best ARM Cortex-A53/A7/A9 Embedded
Design Service Partner for SMIC 40nm/28nm Processes

YouSecure & YouCrypto

SECURITY/CRYPTO APPLICATION



SECURITY/CRYPTO IP SOLUTION

Secured System-on-Chips(SoC)

Proven Root-of-Trust for use in ASICs

- **Secure boot**
  - Execute authenticated and trusted software
  - Prevent malicious code execution
- **Authenticate your code at run-time**
- **Secure software update(Field upgradable)**
- **Anti-rollback protection**

Secure Storage of Secret Information

Confidentially and authenticity is guaranteed

- **Store secret assets**
  - In protected and unprotected storage
- **Confidentiality & authenticity**
  - Achieved with strong cryptographic algorithms
- **Secure key provisioning**
  - Key revocation

Side-channel Attack Protection

Protect against external physical attacks

- **Unique efficiency DPA countermeasures**
  - AES
  - Public Key Accelerator
  - SM4
- **Anti-tampering**
  - Multiple tamper detection mechanisms
  - Configurable depending on treat model
  - Digital Sensors

Device Unique Identity

Prevents counterfeiting and cloning

- **Identify and trust your devices**
  - Uniquely Identify each manufactured part
  - Authenticate your device
- **Device rights management**
- **Attestation**
- **Device decommissioning**

Secure Debugging

Authenticate and protect in-the-field

- **Perform secure failure analysis/RMA**
  - Certificate based
  - Set permissions levels
  - Public key cryptography

Secure Communication

Only using the most secure and latest algorithms

- **TLS/DTLS(TLS/SSL 1.2/1.3)**
- **IPsec and MACsec**
- **Thread networking, Apple HomeKit, Bluetooth, Zigbee and more**

TOOLS AND SUPPORT

- **Provides full integration support**
- **Easy-to-use simulation environment**
- **Standard interfacing**
- **Drivers for software and hardware**
- **Ability to provide full ASIC design/turnkey services**

SECURITY FUNDAMENTAL ELEMENT

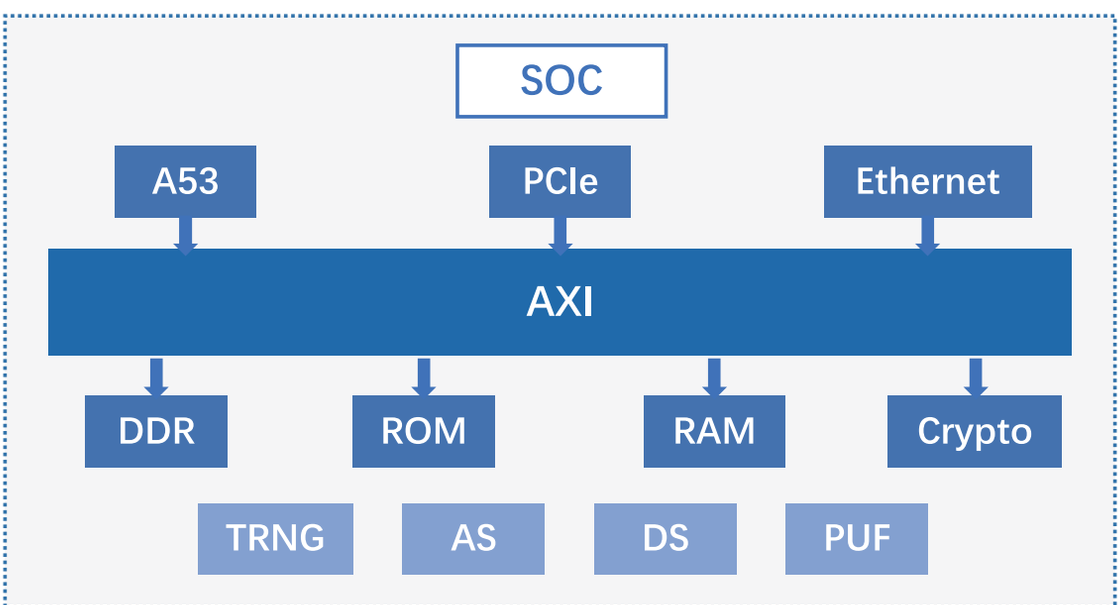
Random Number Generators

- TRNG (NIST 800-90B and AIS-31)
- DRBG (NIST 800-90A/B/C)

Active Shield – AS

Digital Sensor – DS

Physical Unclonable Function - PUF



Security IPs in AP

RICH CRYPTO PORTFOLIO

Asymmetric Algorithms

- RSA/DH /DSA /CRT /ECC /ECDSA/ECDH
  - ECC Curves: NIST, Brainpool, Koblitz, Montgomery, Edwards and others…
- Apple HomeKit/TLS1.3: Curve25519, EdDSA, SRP
- Rabin-Miller (primality check) and Key Generation
- SM2 (OSCCA), EC-KCDSA, ECIES, ECMQV
- SM9 (OSCCA)

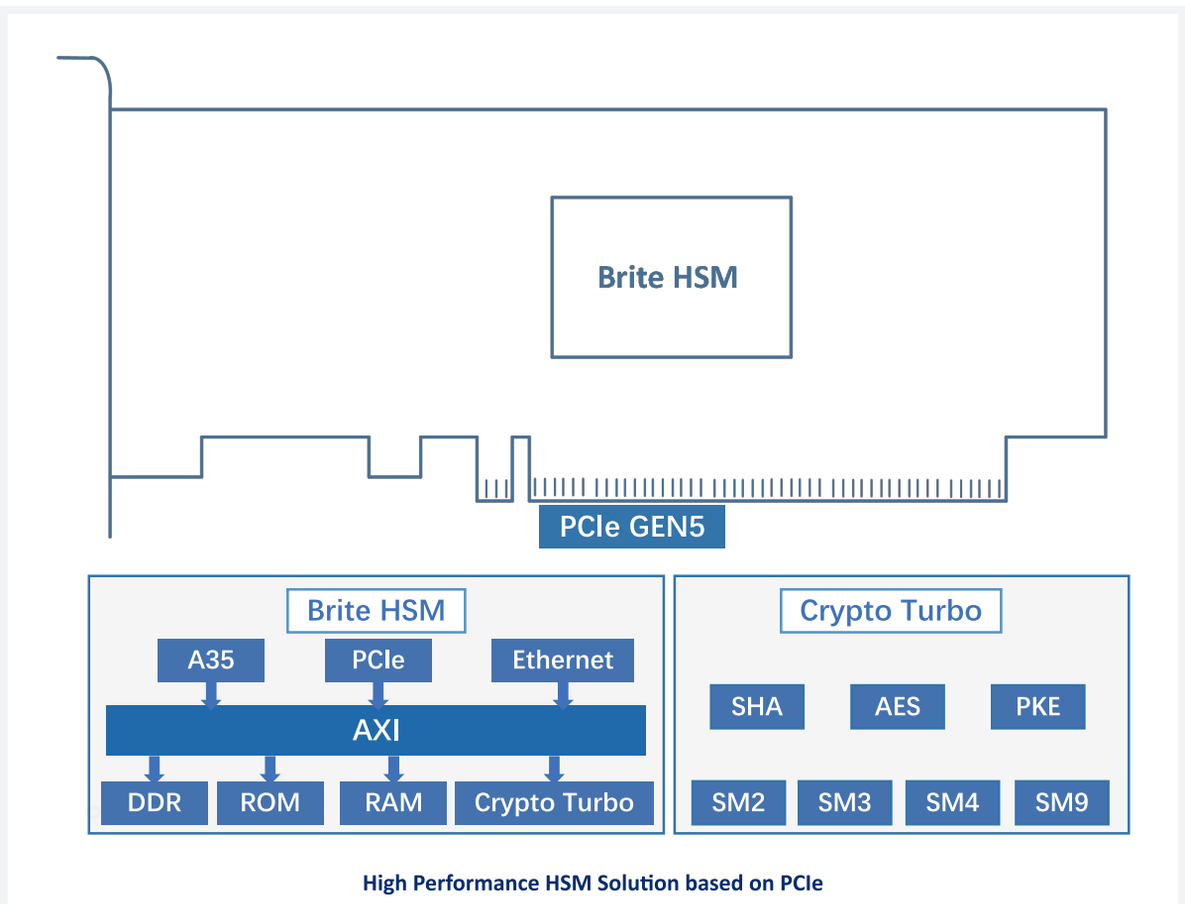
Symmetric Algorithms

- AES/SM4(OSCCA) supporting all modes (GCM, CCM, CFB, CBC…)
- Ultra High-performance AES/SM4(OSCCA)-GCM/CTR/XTS
- Legacy DES/3DES
- Hash-SHA1/2/3, SM3 (OSCCA)

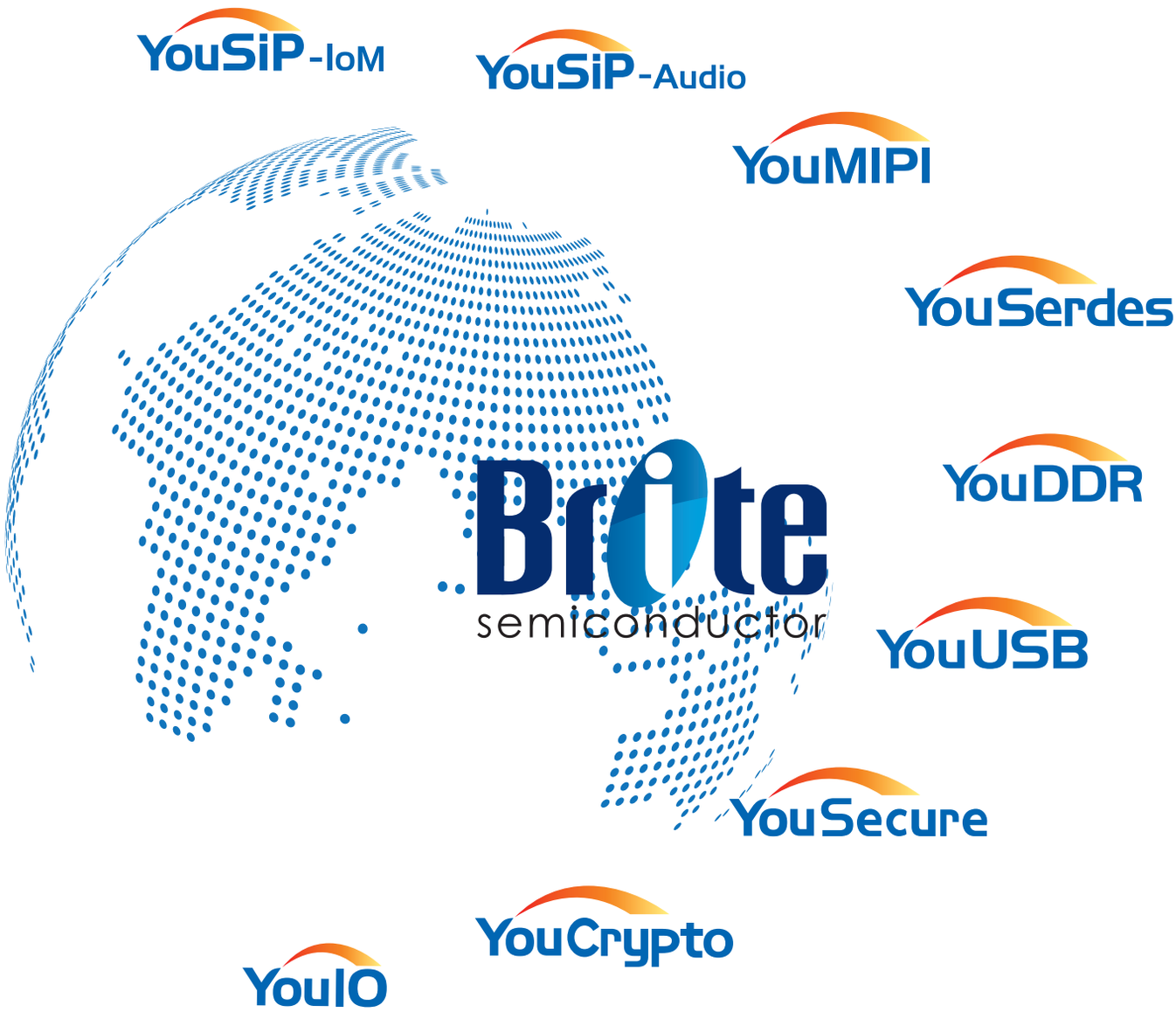
Configurable
Include features as needed

Customizable
Adapt to your specific needs

Scalable
Define performance and footprint depending on your requirement



High Performance HSM Solution based on PCIe


YouSiP-IoM
YouSiP-Audio
YouMIPI
YouSerdes
YouDDR
YouUSB
YouSecure
YouCrypto
YouIO
Brite
semiconductor

Brite semiconductor | 灿芯半导体 Brite Semiconductor

A Leading Custom ASIC & IP Provider



About Brite Semiconductor

Brite Semiconductor is a leading custom ASIC and IP provider, and committed to provide flexible one-stop services from architecture design to chip delivery with high value and differentiated solutions.

Brite Semiconductor provides comprehensive silicon proven “YOU” IP portfolio and YouSiP (Silicon-Platform) solution, which can be widely adopted in 5G, AI, high performance computing, cloud and edge computing, network, IoT, industrial Internet and consumer electronics, etc. YouSiP solution provides a prototype design reference for system house and fabless to speed up the time-to-market.

Founded in 2008, Brite Semiconductor is headquartered in Shanghai, China with four subsidiaries in Hefei, Suzhou, Tianjin and Chendu, and also has sales offices in the US and Taiwan Region.

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